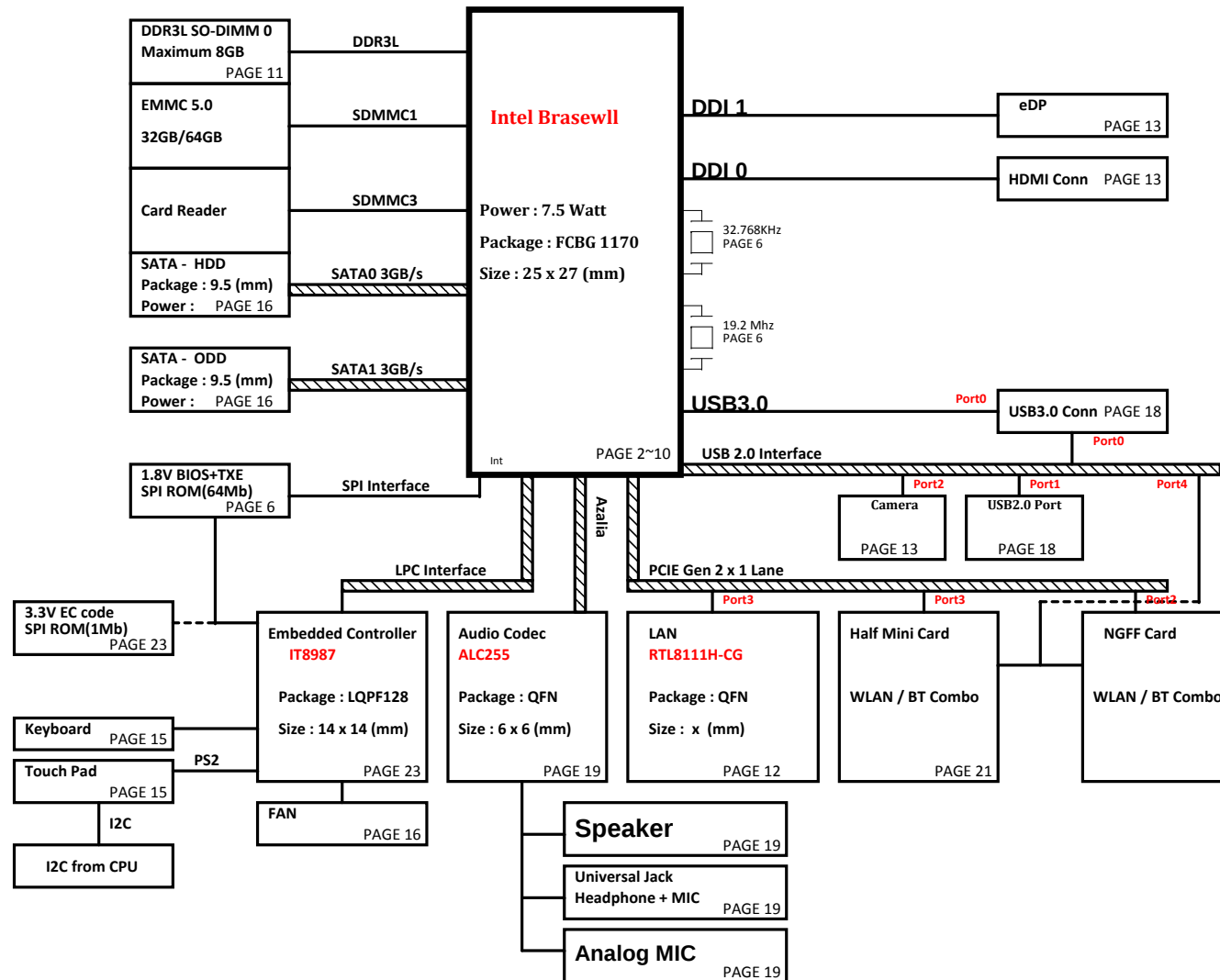


Z8AD UMA(14")

Intel Brasewll Platform Block Diagram

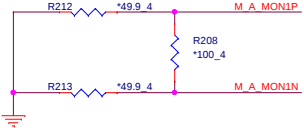
BOM

EM@ : EMMc
 HD@ : HDD
 GS@ : G-sensor
 TPM@ : TPM
 TSI@ : TOUCH SCREEN I2C
 SP@ : Special

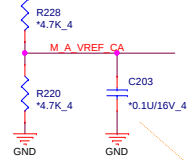


+1.35VSUS [3,9,11,27]
+3V_S5 [3,5,9,12,14,15,16,22,26]

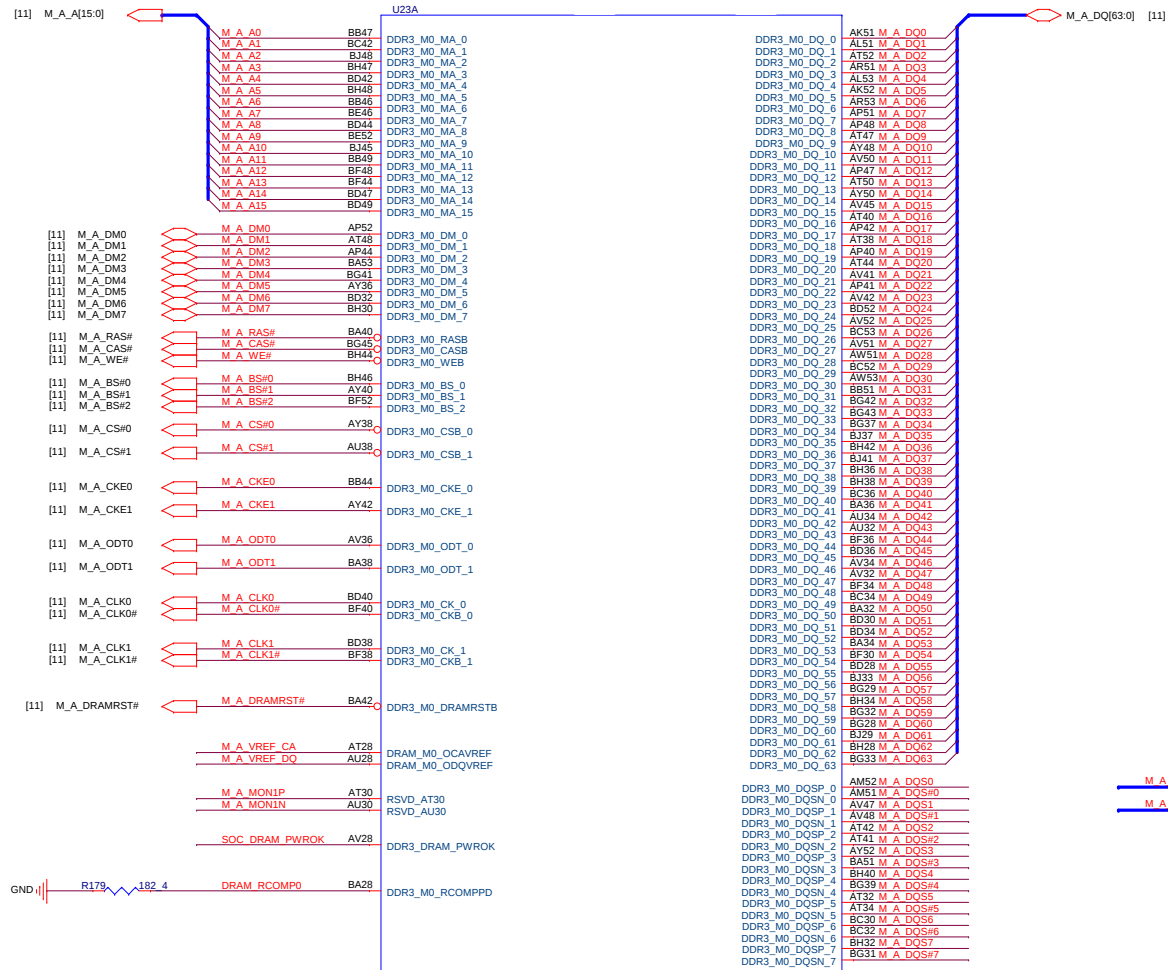
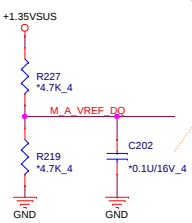
PLACE THE RESISTORS AS CLOSE AS POSSIBLE TO SOC(BSW)
ROUTE THEN AS SINGLE ENDED LINES



ROUTE ALL VREF POWER SIGNALS AS THICK TRACES
PLACE TWO 4.7K RESISTORS CLOSE TO CPU PINS ON M_VREF
ROUTE THE VREF POWER SIGNALS WITH THICK TRACES

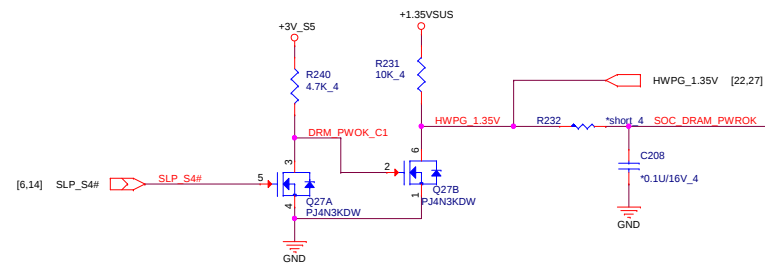


PLACE 0.1UF CAP CLOSE TO CPU



Channel 0	Channel 1	SoC Supported Memory Operation Speed
1333 MHz	X	1066 MHz
1600 MHz	X	1600 MHz
1333 MHz	1333 MHz	1066 MHz
1600 MHz	1600 MHz	1600 MHz

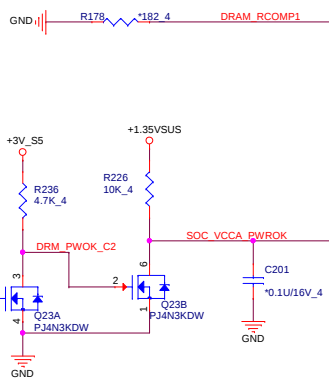
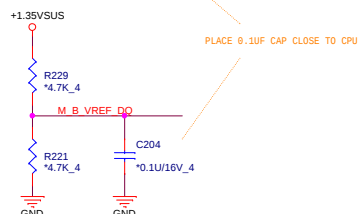
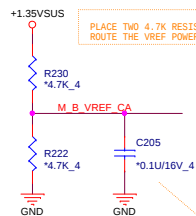
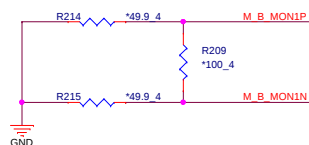
Channel 0 need to be populated first for the platform to power on





Quanta Computer Inc.
PROJECT : Z8AD

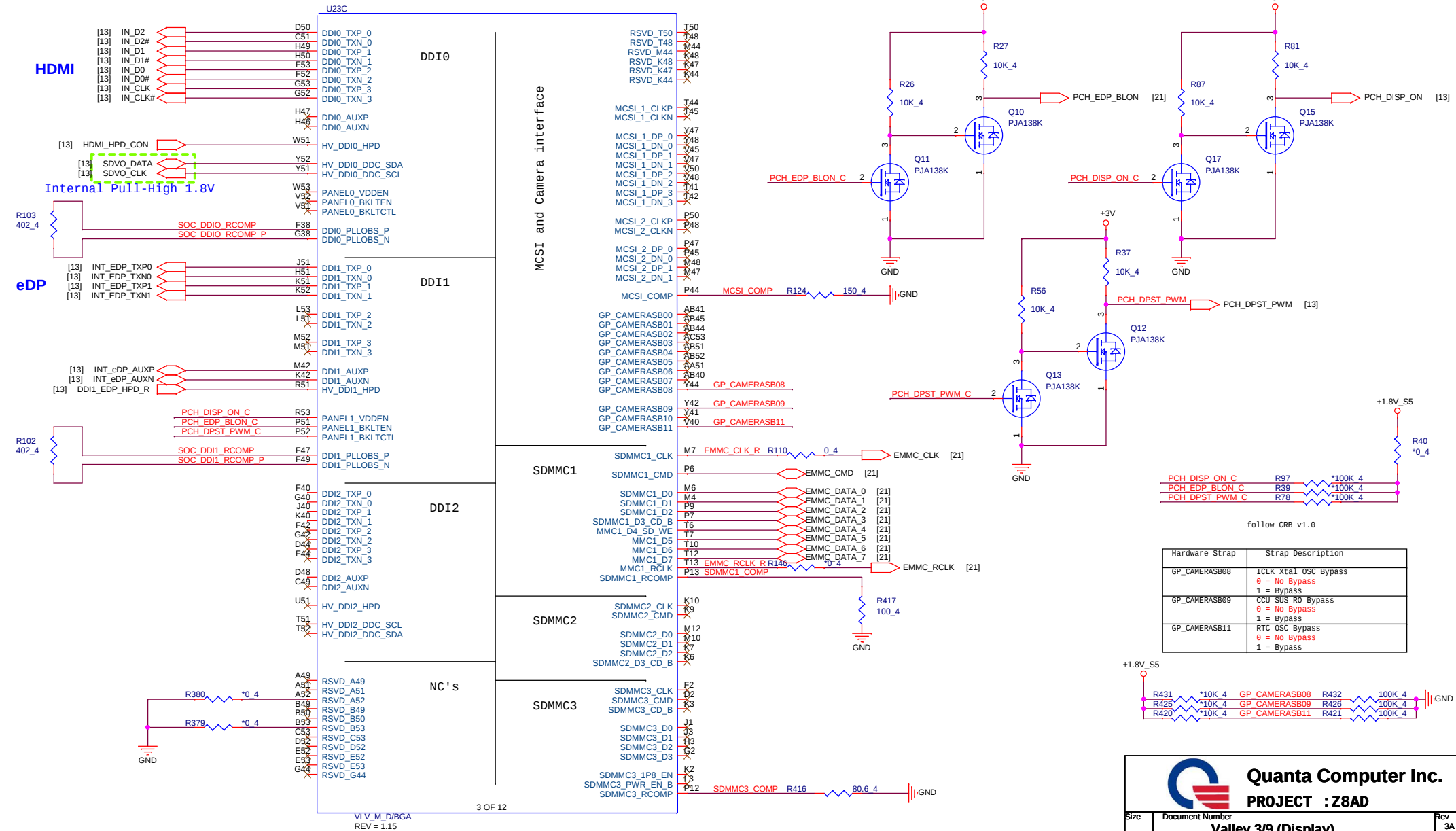
Size	Document Number	Rev
	Valley 1/9 (DDRA)	3A
Date:	Wednesday, April 08, 2015	Sheet 2 of 32



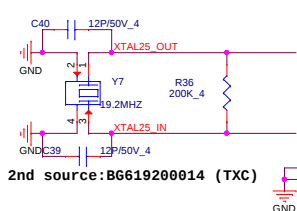
U238			
BB7	DDR3_M1_MA_0		AK3
BC12	DDR3_M1_MA_1		AK3
BI0	DDR3_M1_MA_2		AK2
BD12	DDR3_M1_MA_3		AK1
BH6	DDR3_M1_MA_4		AK2
BB8	DDR3_M1_MA_5		AK1
BB8	DDR3_M1_MA_6		AK1
BD10	DDR3_M1_MA_7		AK1
BB5	DDR3_M1_MA_8		AK7
BI0	DDR3_M1_MA_9		AK6
BB6	DDR3_M1_MA_10		AK4
BF9	DDR3_M1_MA_11		AK7
BF10	DDR3_M1_MA_12		AK7
BD0	DDR3_M1_MA_13		AK4
BD0	DDR3_M1_MA_14		AK9
BD0	DDR3_M1_MA_15		AK4
AP2	DDR3_M1_DM_0		AK12
AT6	DDR3_M1_DM_1		AK16
AP10	DDR3_M1_DM_2		AK14
BC13	DDR3_M1_DM_3		AK10
AG15	DDR3_M1_DM_4		AK13
BD22	DDR3_M1_DM_5		AK12
BH28	DDR3_M1_DM_6		AK2
	DDR3_M1_DM_7		AK2
BA14	DDR3_M1_RASB		AK1
BH10	DDR3_M1_CASB		AK3
BD0	DDR3_M1_WEB		AK3
BH8	DDR3_M1_BS_0		AK1
AY12	DDR3_M1_BS_1		AK12
BF0	DDR3_M1_BS_2		AK11
AY16	DDR3_M1_CSB_0		AK11
AU16	DDR3_M1_CSB_1		AK12
BB10	DDR3_M1_CKE_0		AK18
AY12	DDR3_M1_CKE_1		AK18
AV18	DDR3_M1_ODT_0		AK18
BA16	DDR3_M1_ODT_1		AK20
BD14	DDR3_M1_CK_0		AK20
BF16	DDR3_M1_CKB_0		AK24
BD16	DDR3_M1_CK_1		AK28
BF16	DDR3_M1_CKB_1		AK28
BA12	DDR3_M1_DRAMRSTB		AK22
AT26	DDR3_M1_OCAVREF		AK26
AU26	DDR3_M1_ODQVREF		AK26
AT24	RSVD_AT24		AK22
AU24	RSVD_AU24		AK22
AV26	DDR3_DRAM_PWROK		AK2
BA26	DDR3_M1_ROMPPD		AK2
		DDR3_M1_DQSP_0	AK2
		DDR3_M1_DQSN_0	AK7
		DDR3_M1_DQSP_1	AK6
		DDR3_M1_DQSN_1	AK13
		DDR3_M1_DQSP_2	AK2
		DDR3_M1_DQSN_2	AK3
		DDR3_M1_DQSP_3	AK14
		DDR3_M1_DQSN_3	AK2
		DDR3_M1_DQSP_4	AK22
		DDR3_M1_DQSN_4	AK22
		DDR3_M1_DQSP_5	AK20
		DDR3_M1_DQSN_5	AK22
		DDR3_M1_DQSP_6	AK22
		DDR3_M1_DQSN_6	AK22
		DDR3_M1_DQSP_7	AK23
		DDR3_M1_DQSN_7	AK23

2 OF 12

VLV_M_D/BGA
REV = 1.15



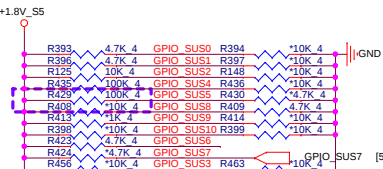




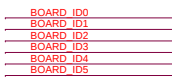
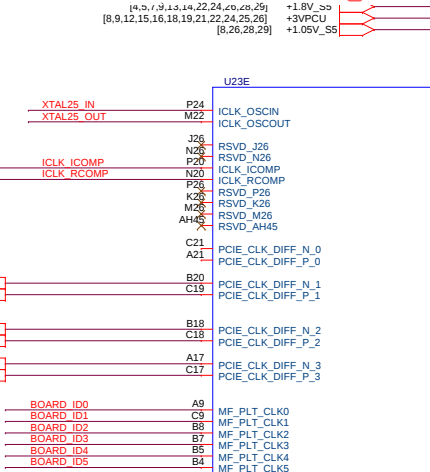
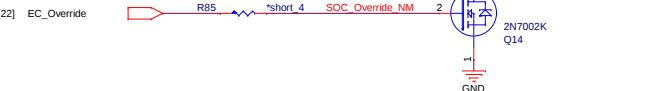
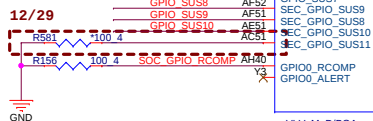
2nd source: BG619200014 (TXC)

NGFF
WLAN
LAN

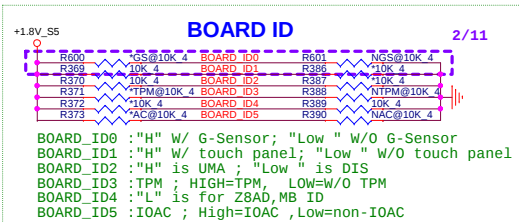
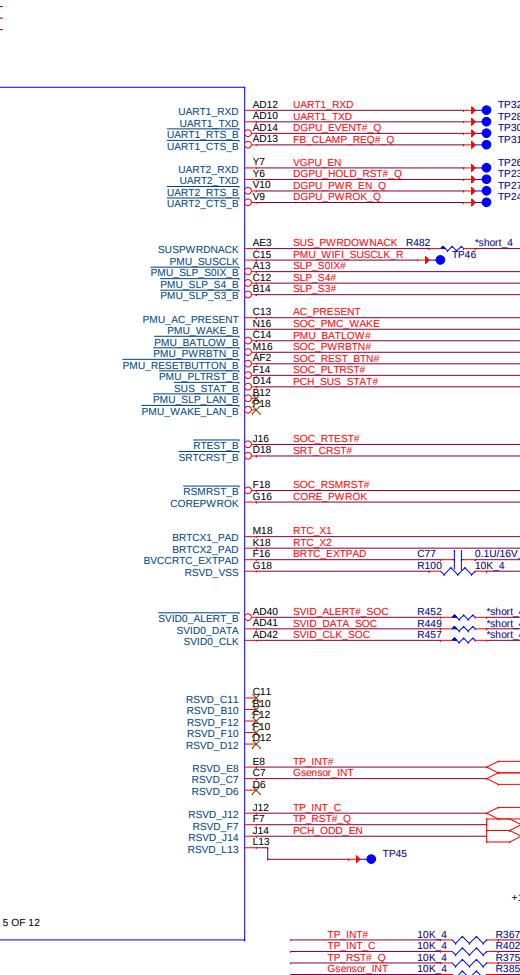
Hardware Strap	Strap Description
GPIO_SUS[0]	0 = 0010 not detected 1 = 0010 detected
GPIO_SUS[1]	0 = 0011 not detected 1 = 0011 detected
GPIO_SUS[2]	Top Swap(A18 Override) 0 = Change Boot Loader address 1 = Normal Operation
GPIO_SUS[4]	BDUS Boot Selection 0 = No SPI 1 = SPI
GPIO_SUS[5]	Security Flash Descriptors 0 = Override 1 = Normal Operation
GPIO_SUS[8]	ICLK_USB 2.0, 001 SFR supply select 0 = Supply is 1.25V 1 = Supply is 1.35V
GPIO_SUS[9]	ICLK_USB 2.0, 001 SFR Bypass 0 = No bypass 1 = Bypass with 1.05V (Internal PU)
GPIO_SUS[10]	PMOS Select 0 = Fuse controller 1 = PMC (Internal PU)



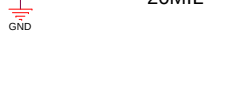
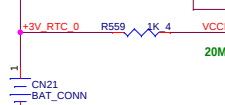
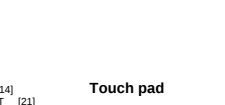
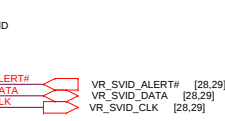
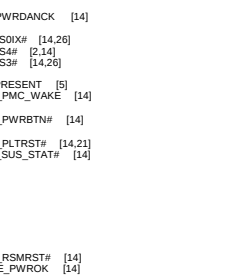
11/28 modify



5 OF 12

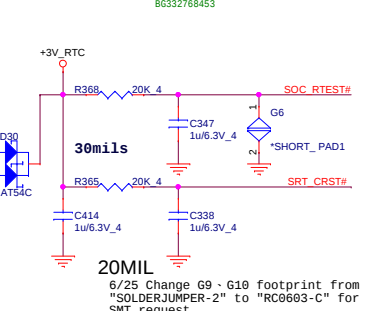
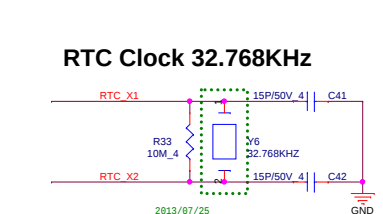
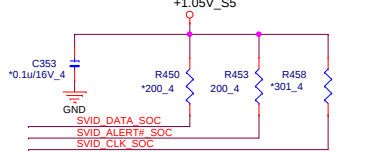
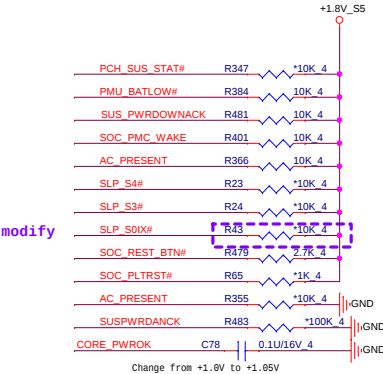


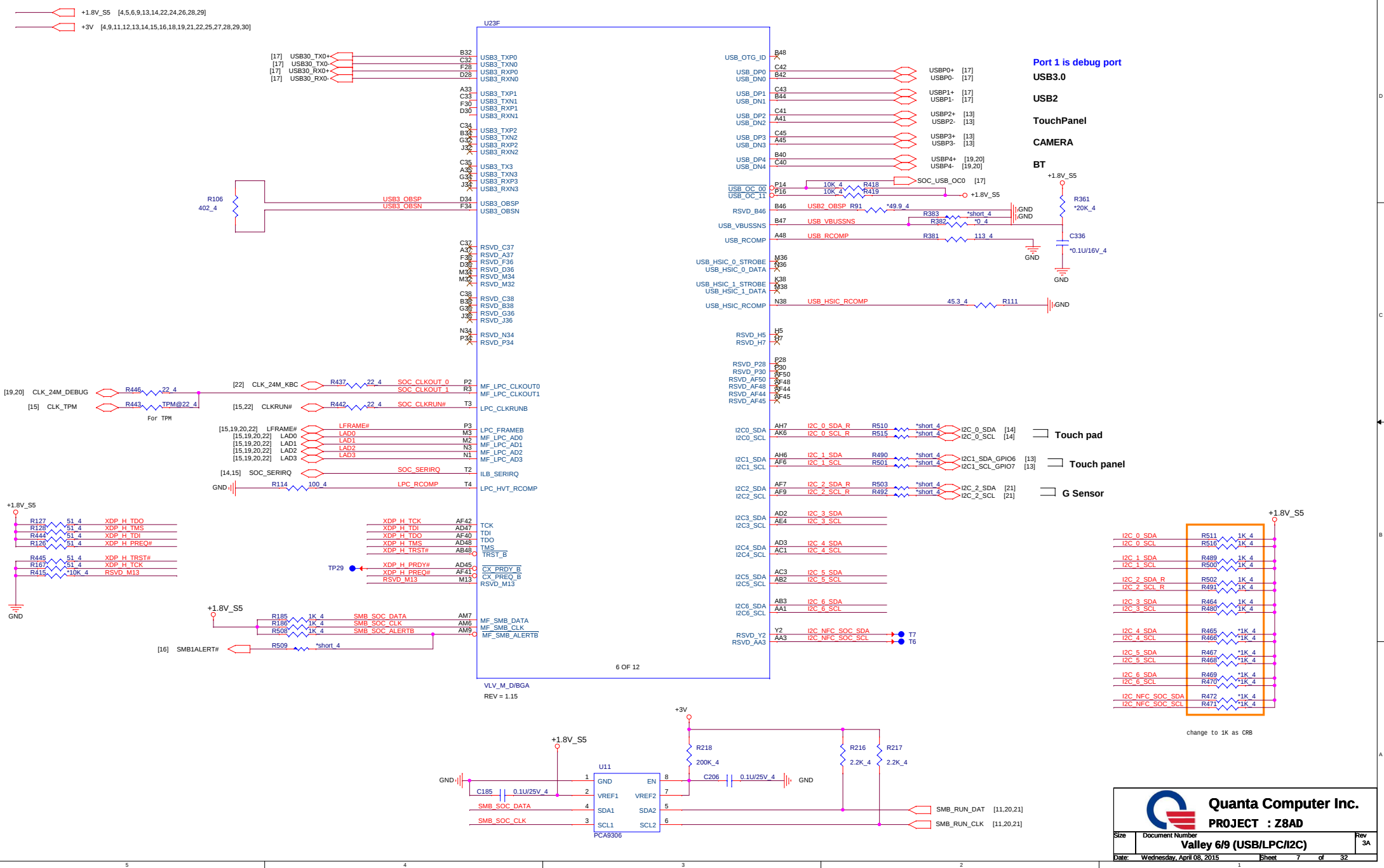
BOARD_ID0 : "H" W/ G-Sensor; "Low" W/O G-Sensor
BOARD_ID1 : "H" W/ touch panel; "Low" W/O touch panel
BOARD_ID2 : "H" is UMA; "Low" is DIS
BOARD_ID3 : TPM; HIGH=TPM, Low=W/O TPM
BOARD_ID4 : "L" is for Z8AD, MB ID
BOARD_ID5 : IOAC; High=IOAC, Low=non-IOAC

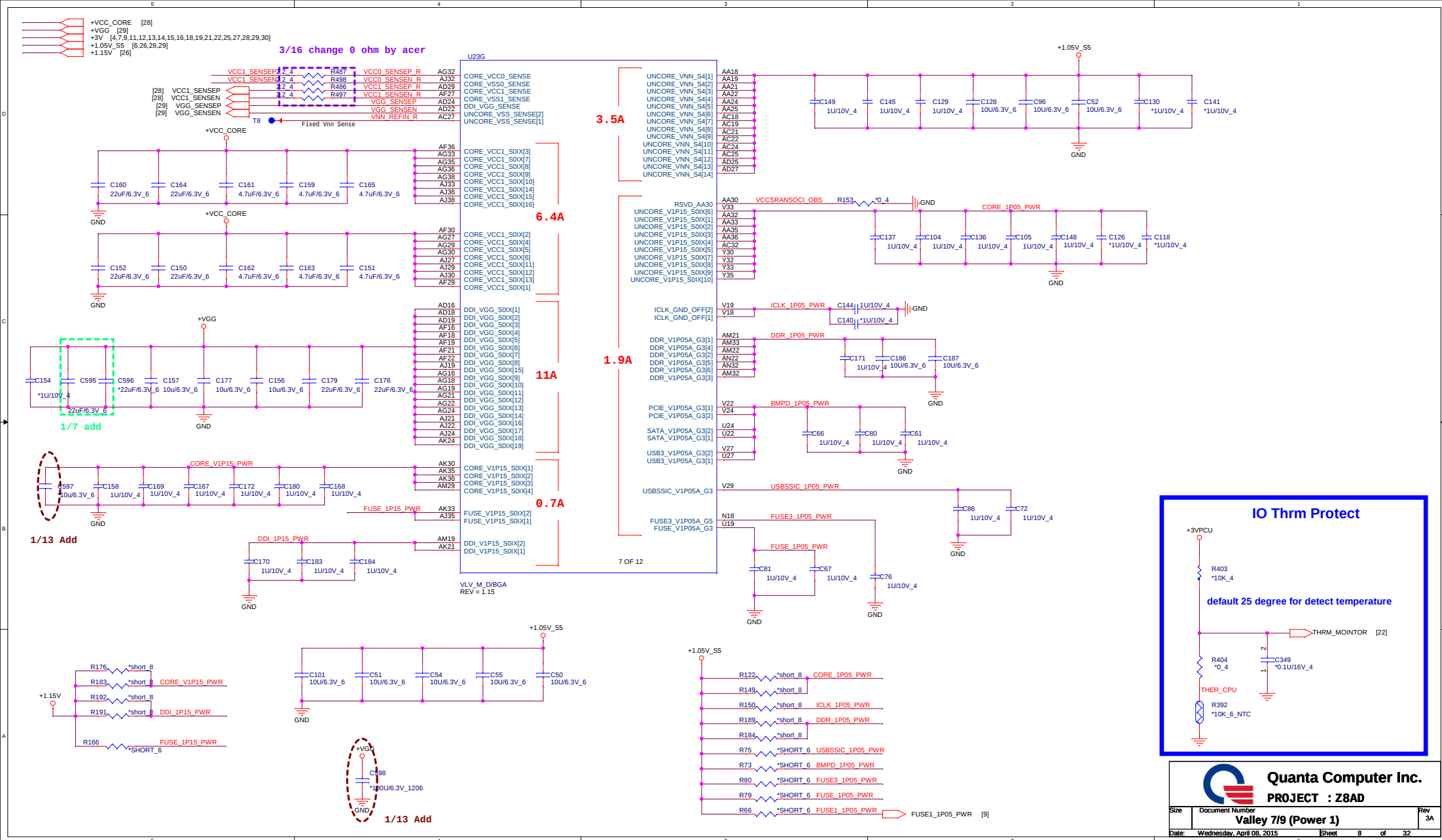


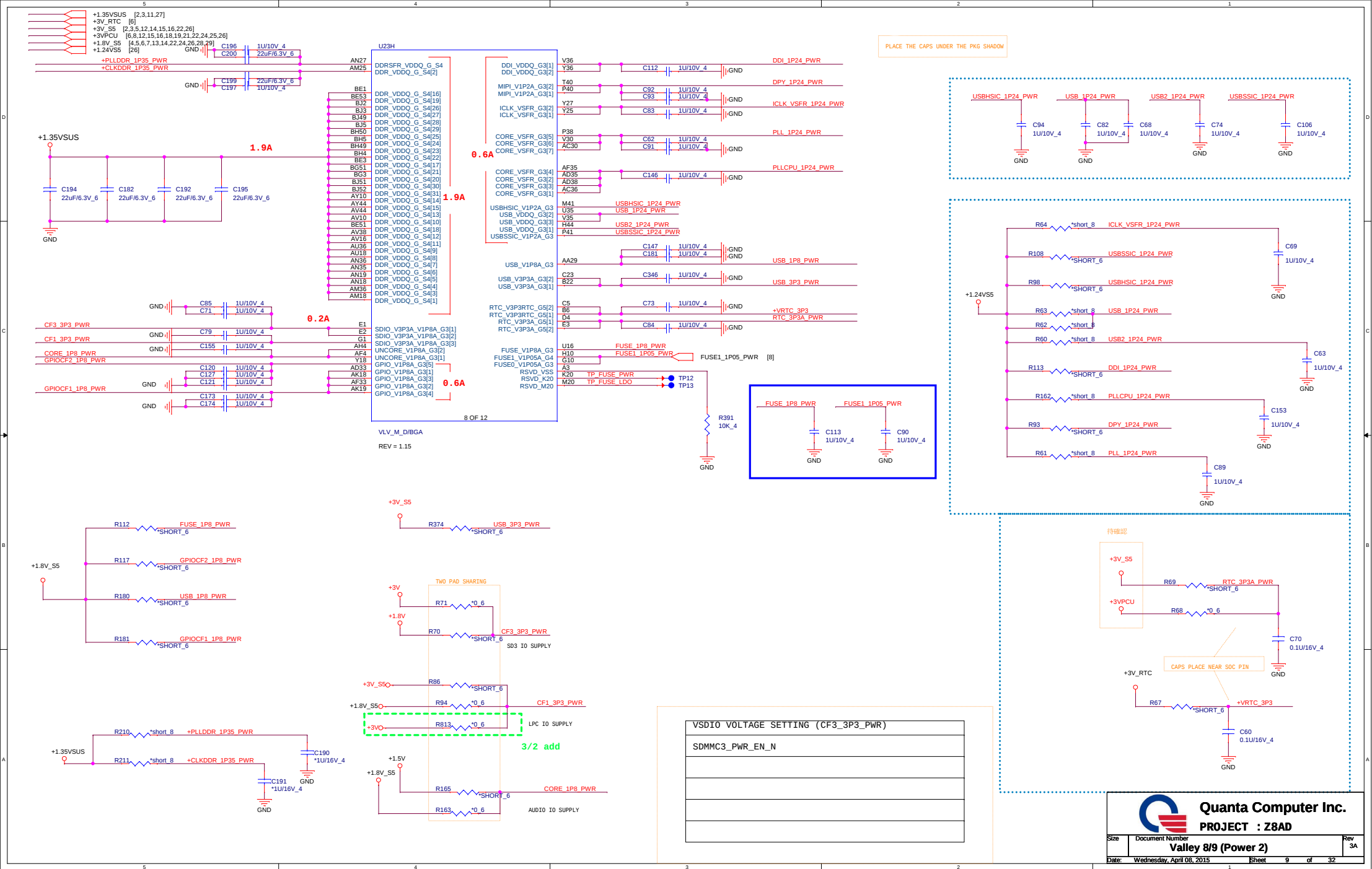
11/28 modify

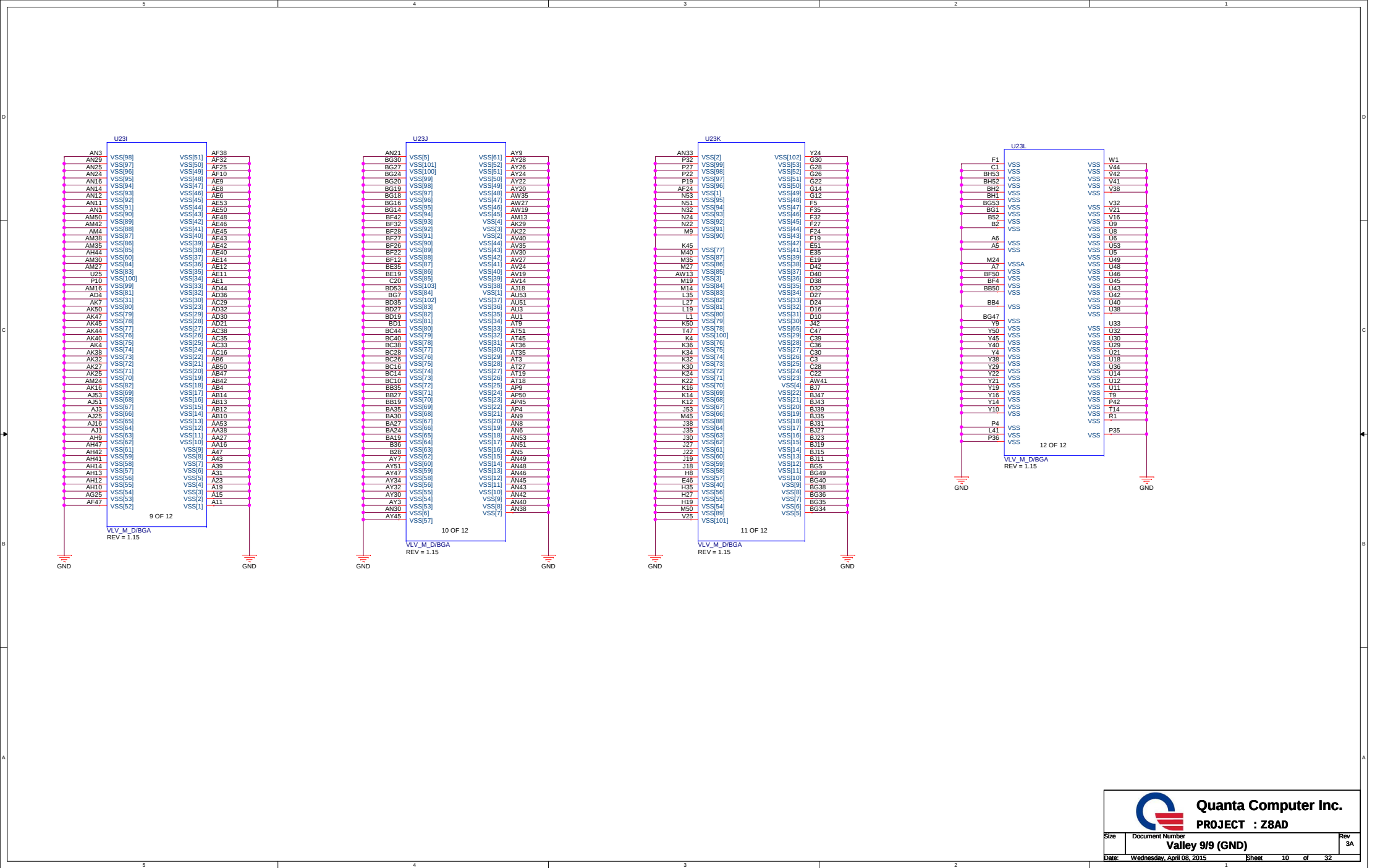
11/26 modify







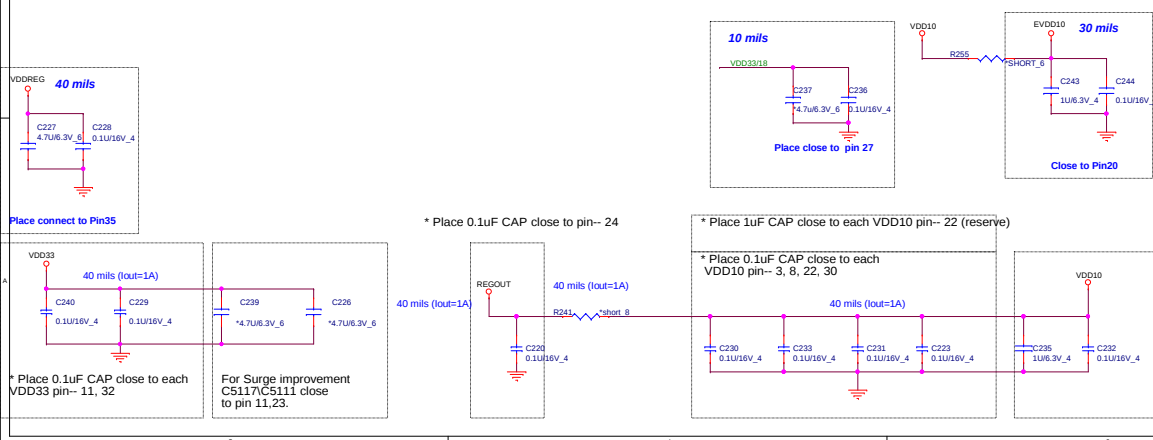
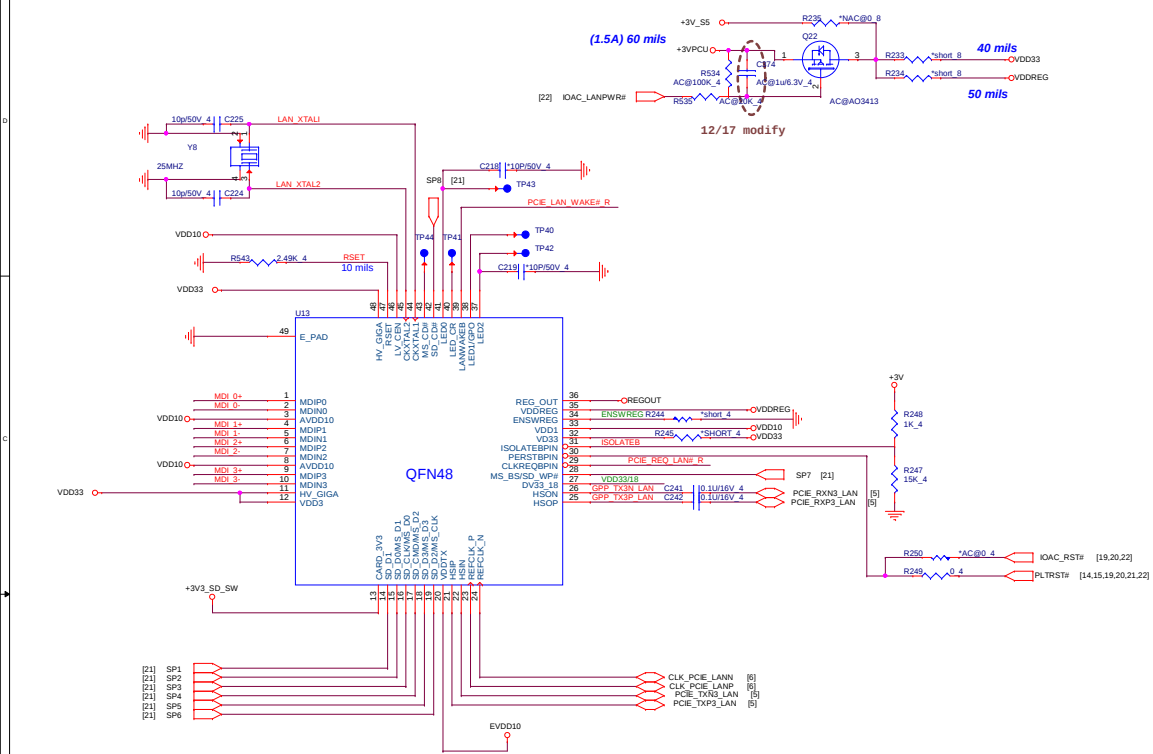
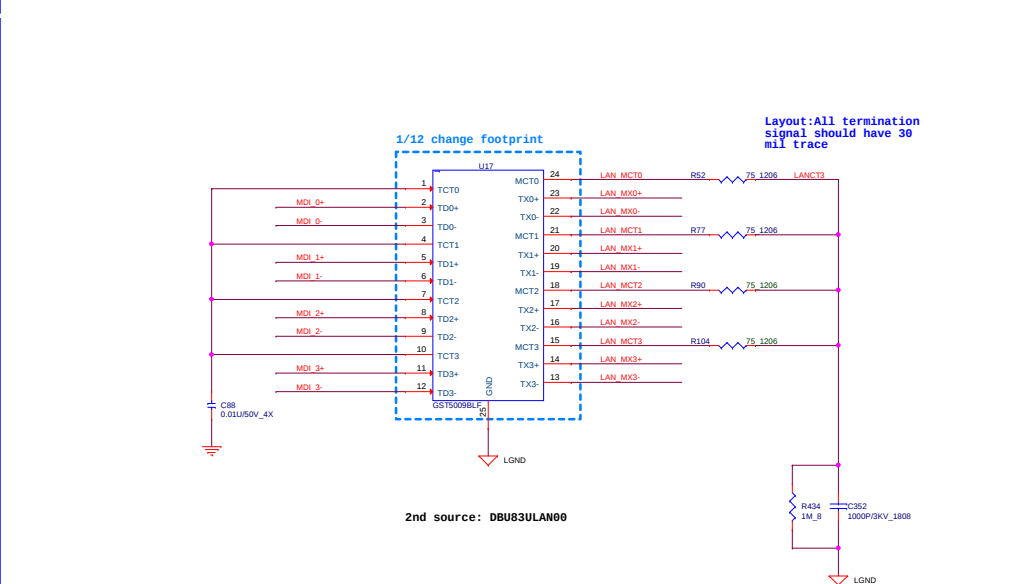




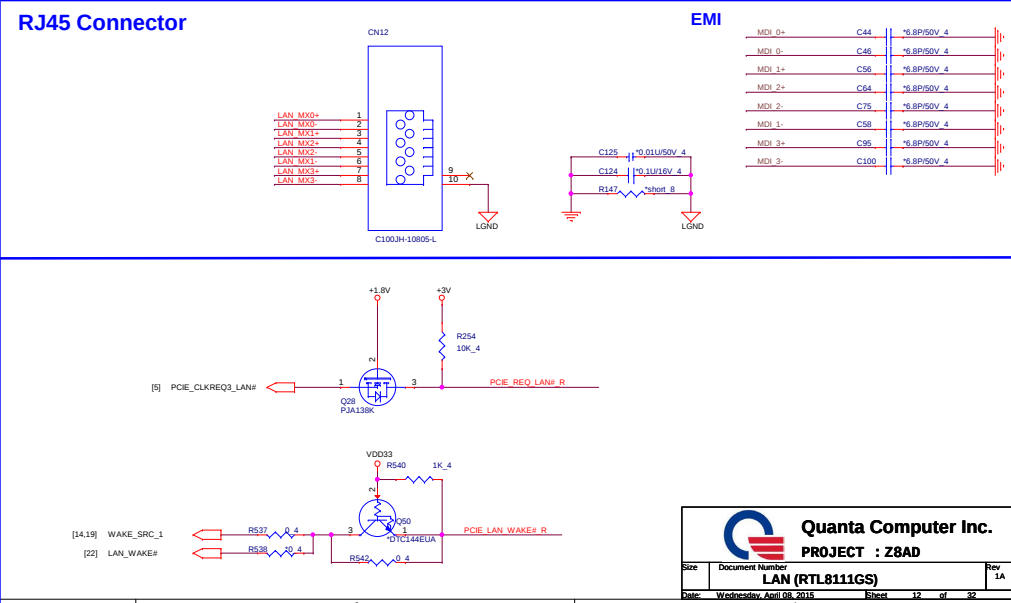
Quanta Computer Inc.
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	Valley 9/9 (GND)	3A
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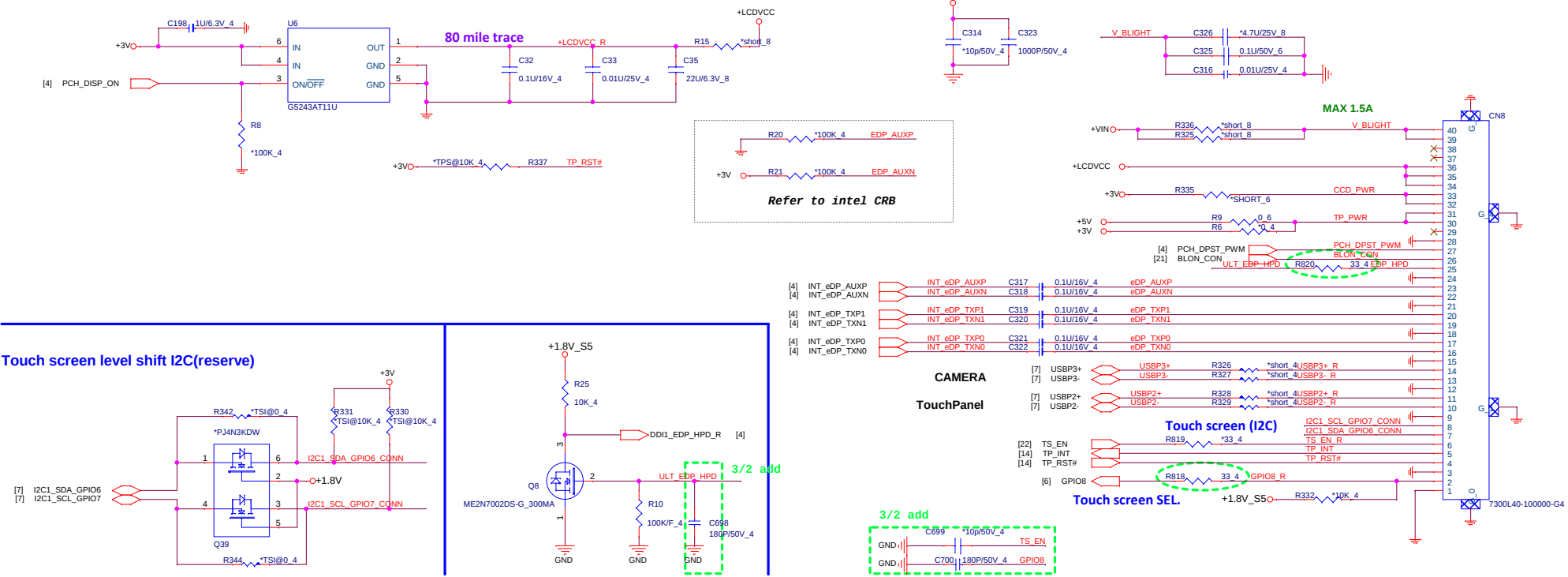
LAN/Card reader (LAN)

Transfer A'' 

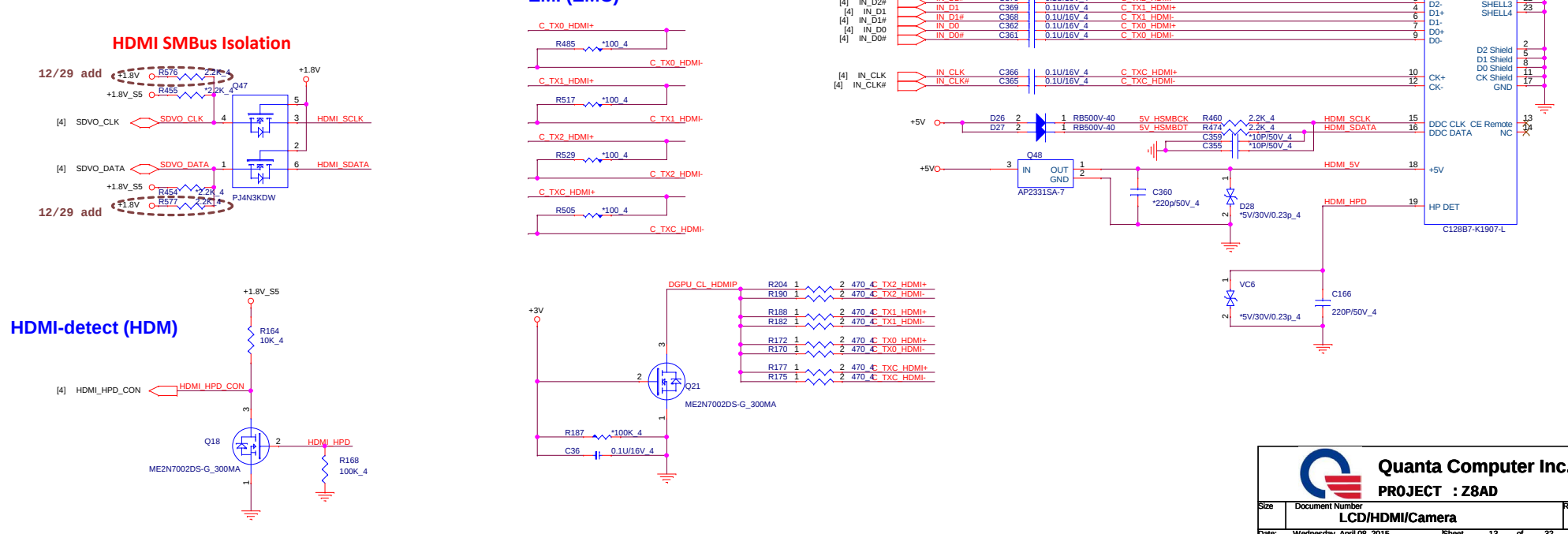
RJ45 Connector

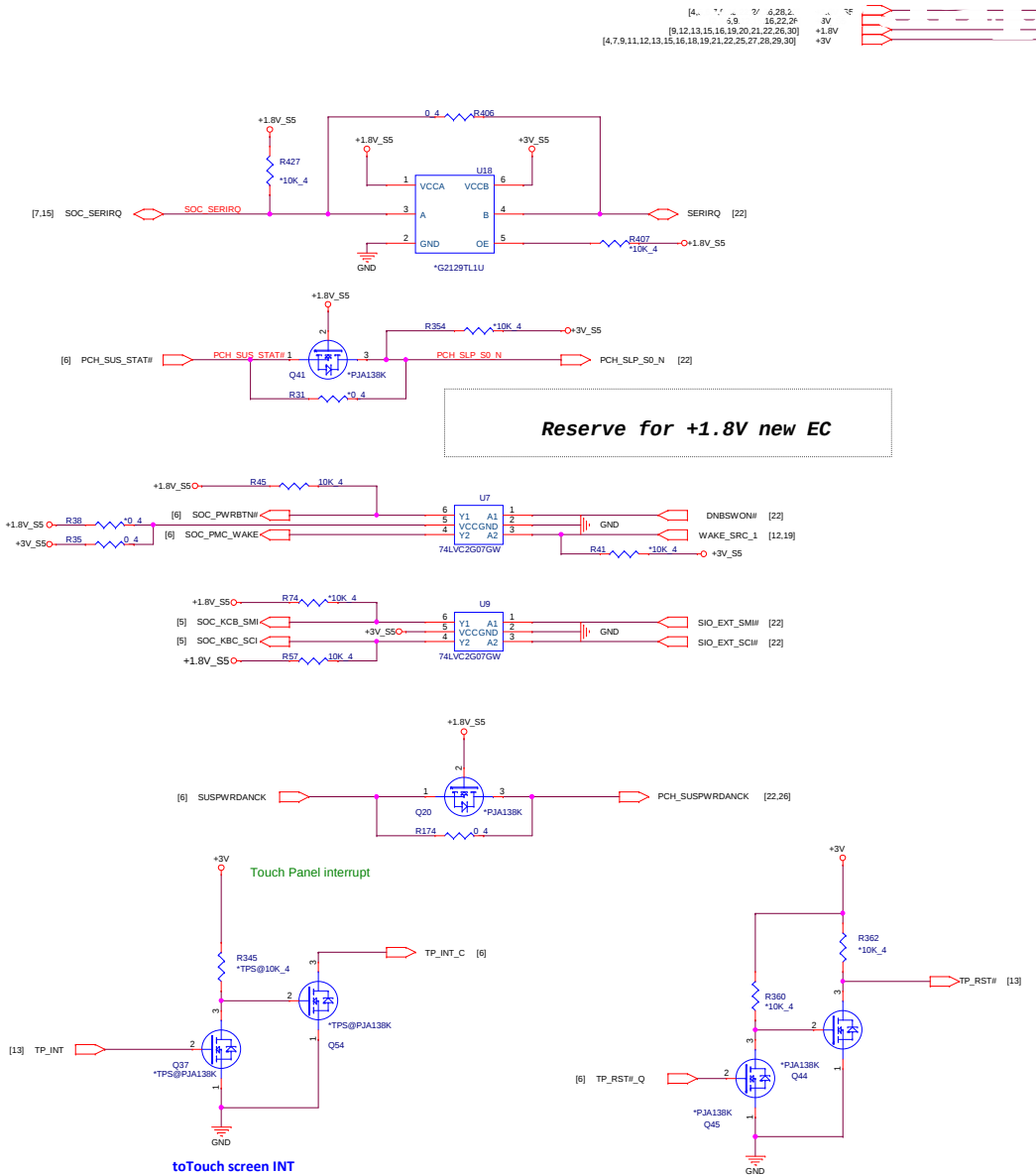


LCD POWER SWITCH

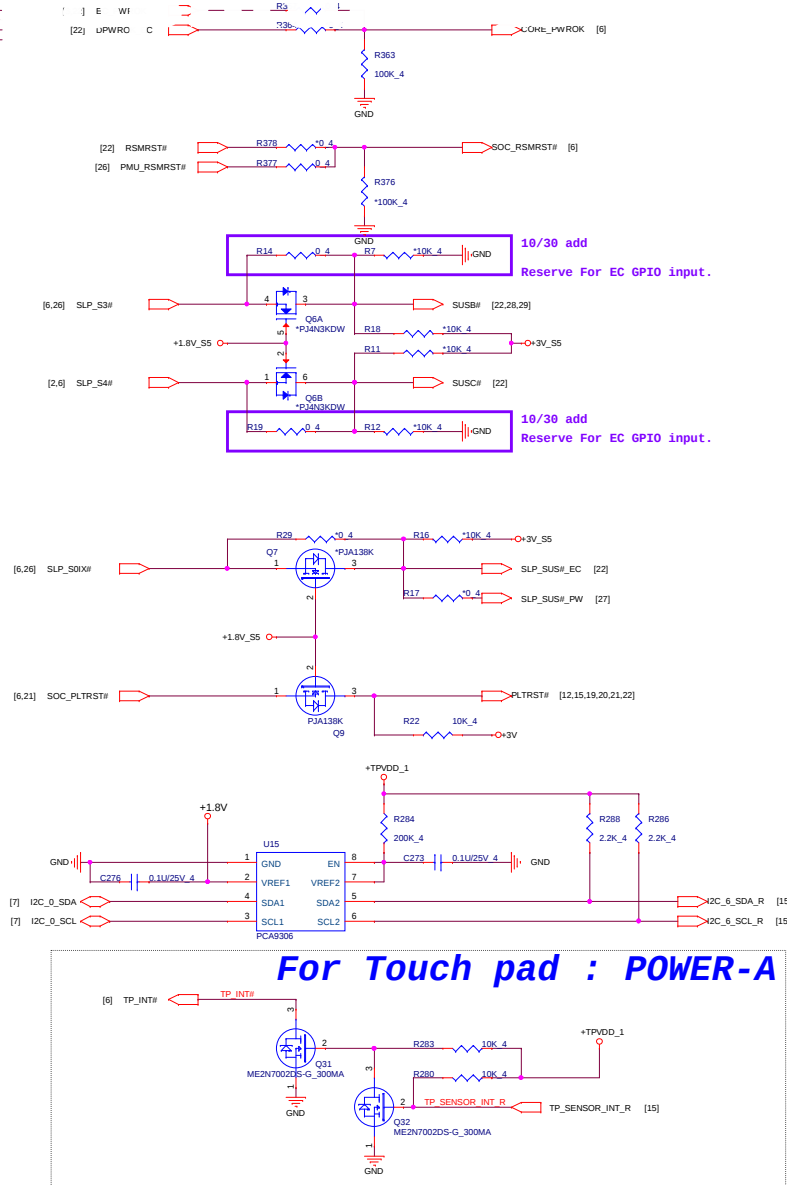


HDMI Conn.

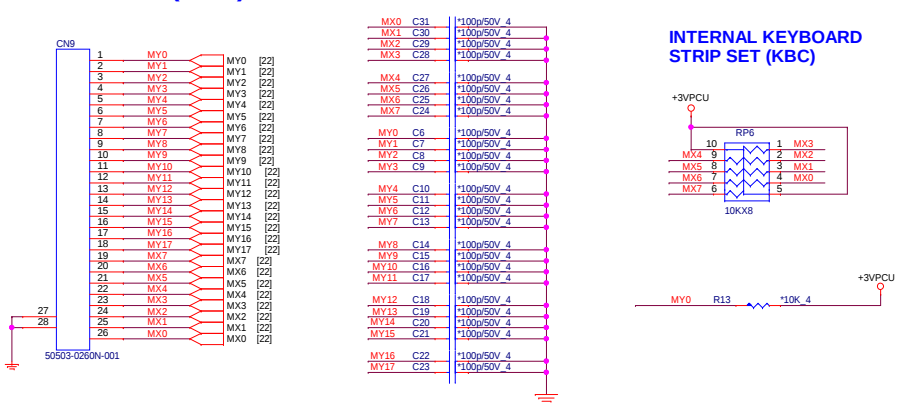




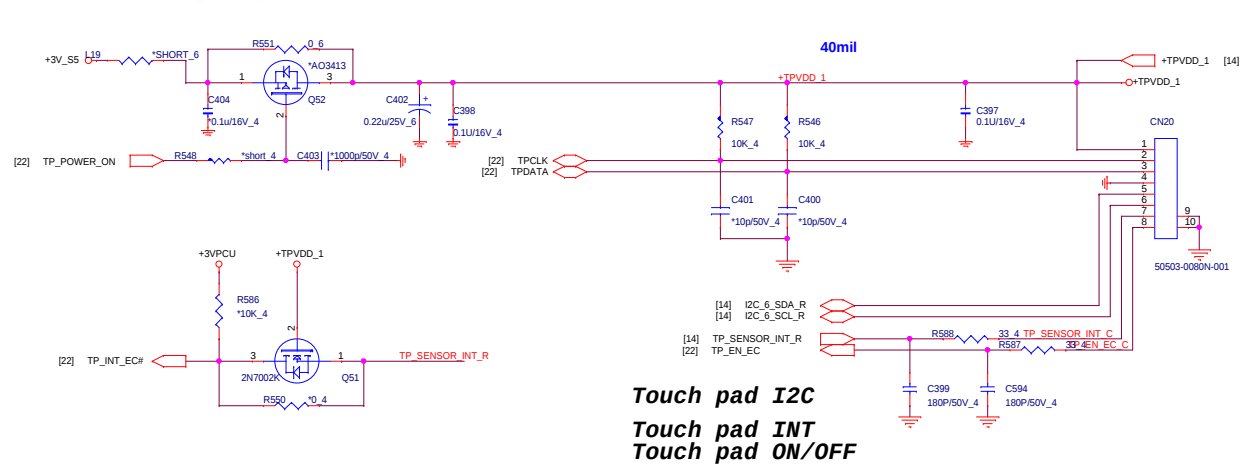
3/2 Del



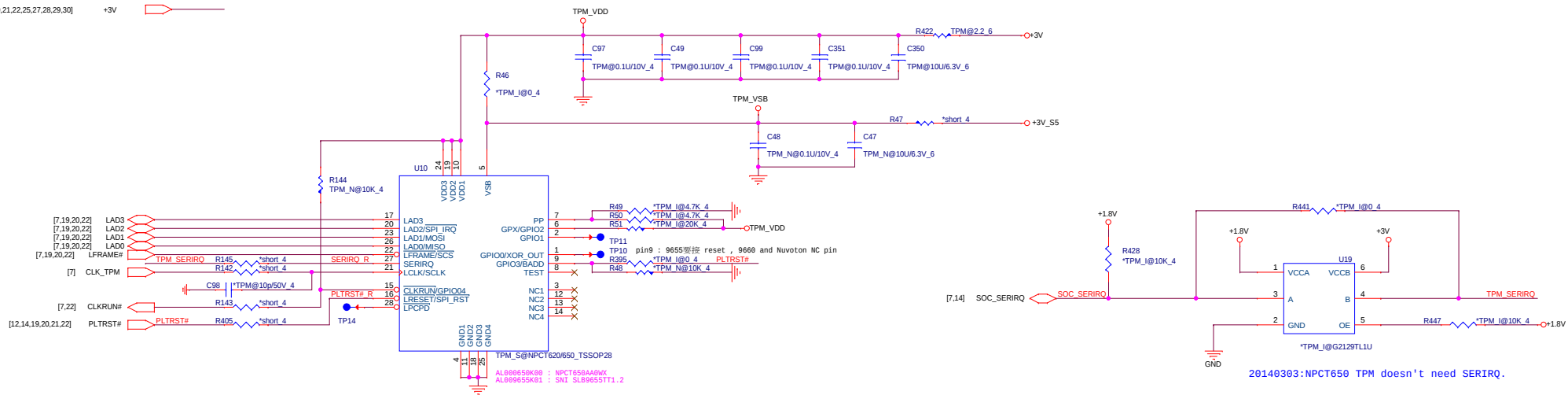
KEYBOARD (KBC)



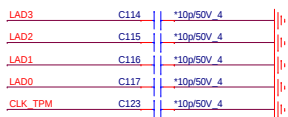
PROCESO AD (PFA)



TPM (TPM)



20140303:NPCT650 TPM doesn't need SERIRQ.



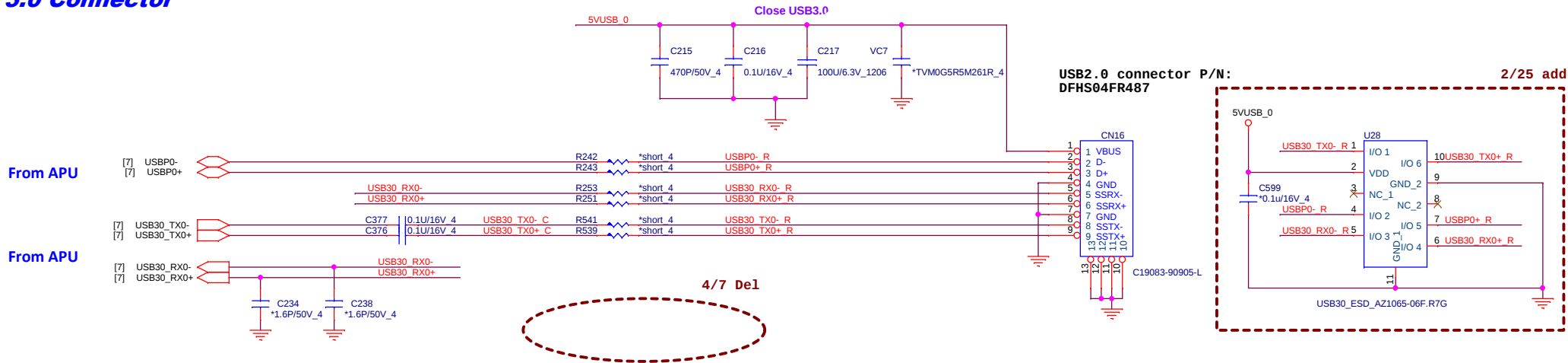
```
TPM_N for 新唐
TPM_I for 英飛凌--- default
```



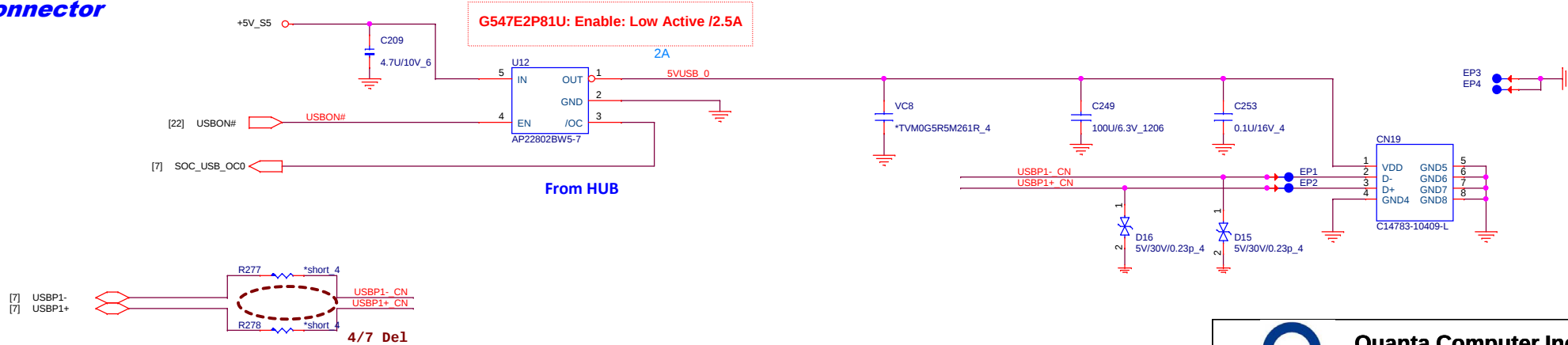
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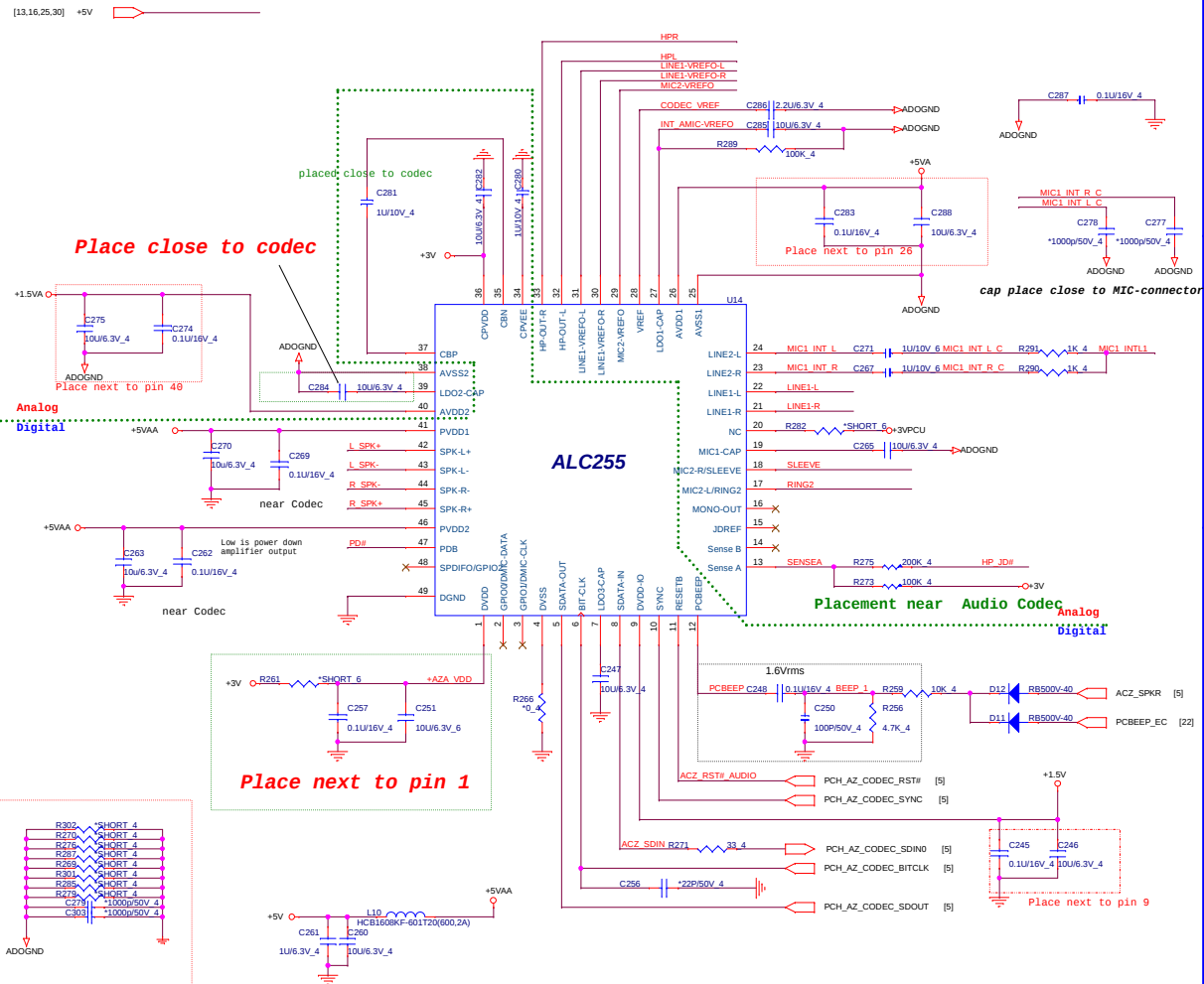
USB 3.0 Connector



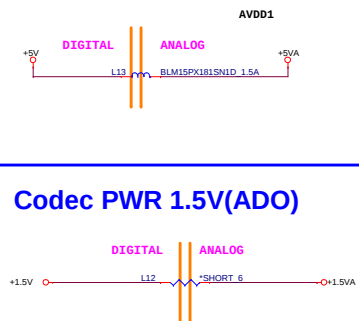
USB 2.0 Connector



Codec(ADO)



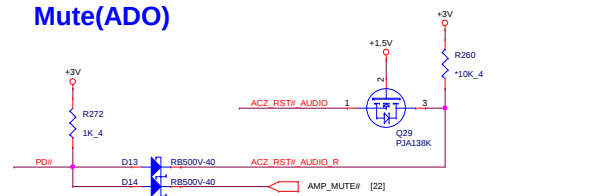
Codec PWR 5V(ADO)



Codec PWR 1.5V(ADO)

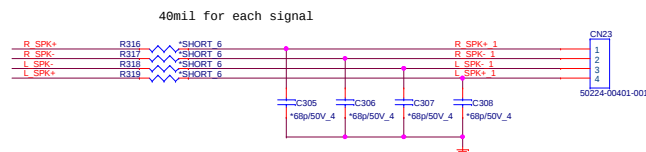


Mute(ADO)

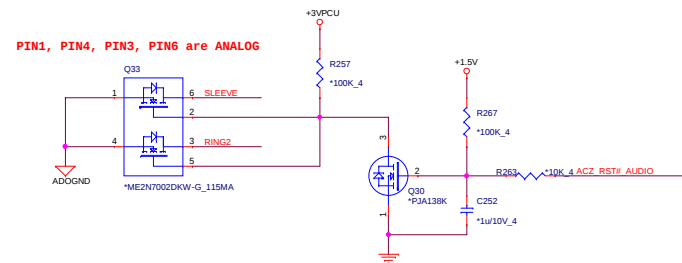


Internal Speaker

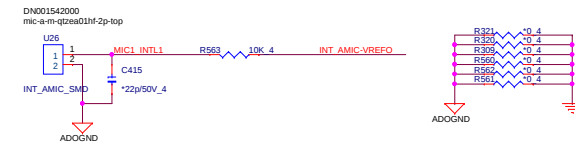
footprint 88266-040xx-xxx-4p-1



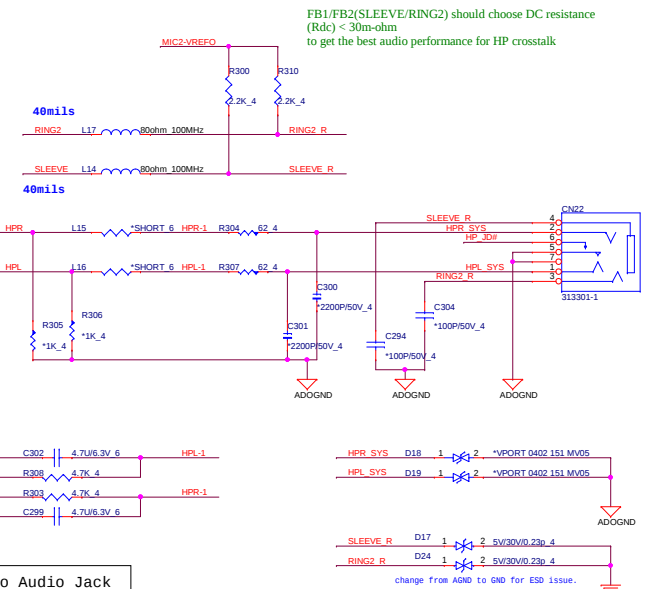
circumlig circle (AF 0)



INT MIC array

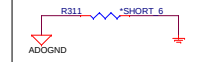


HEADPHONE/MIC/LINE combo



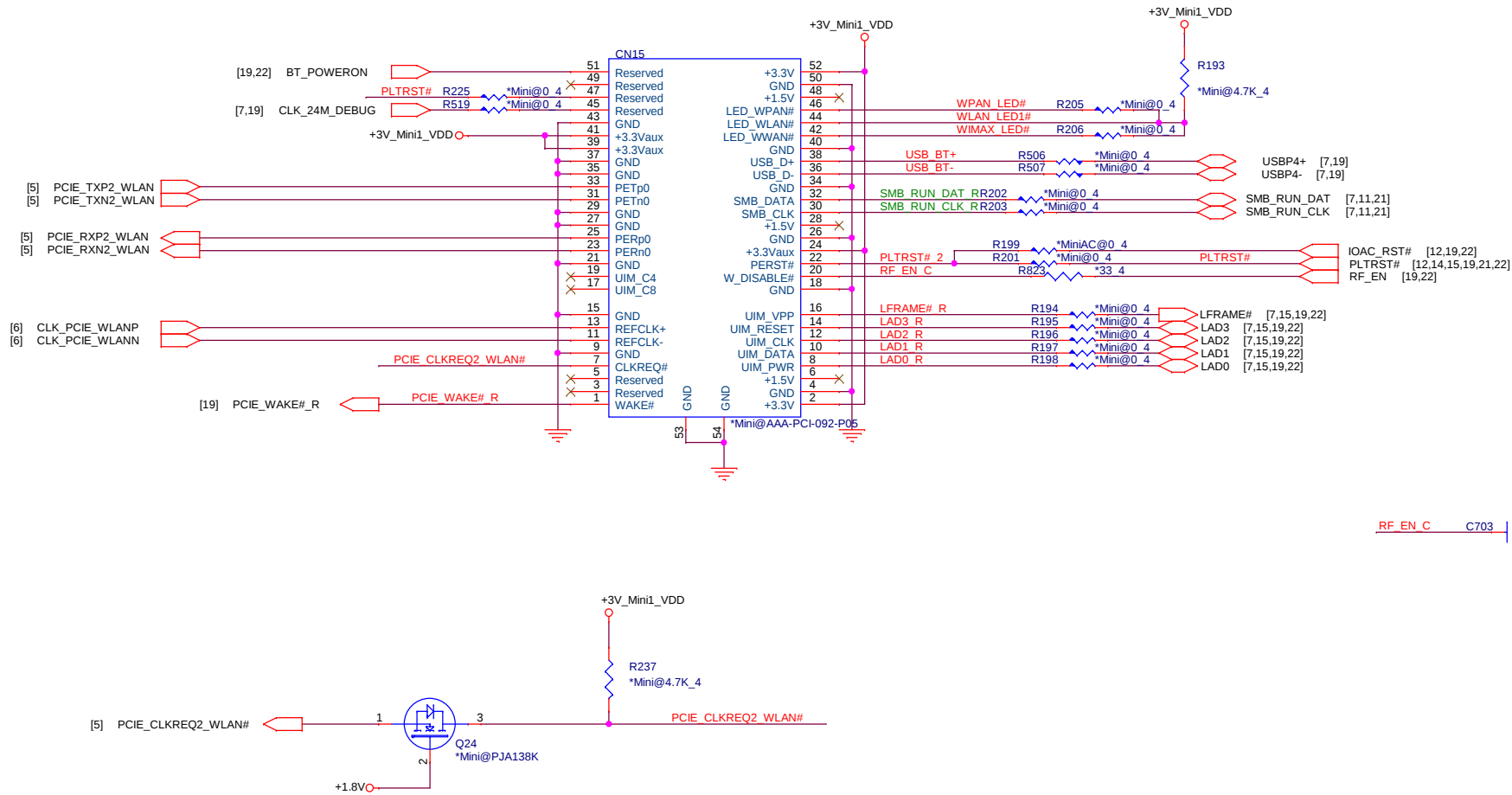
FB1/FB2(SLEEVE/RING2) should choose DC resistance (Rdc) < 30m-ohm
to get the best audio performance for HP crosstalk

Close to Audio Jack

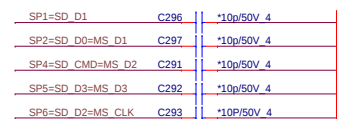
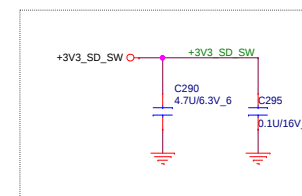
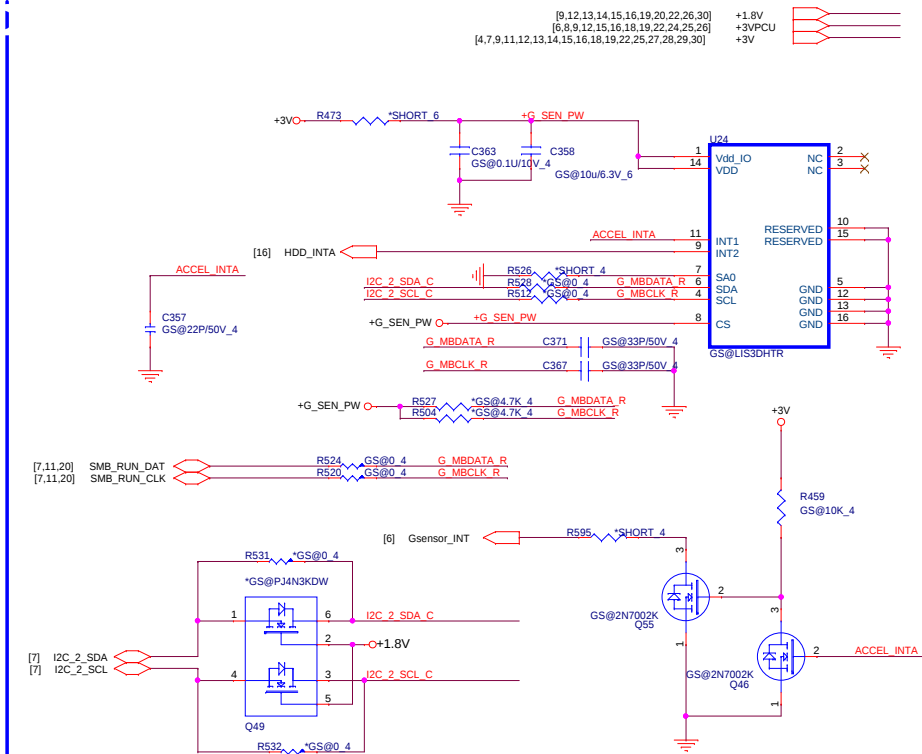


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	USB HUB -1	1A
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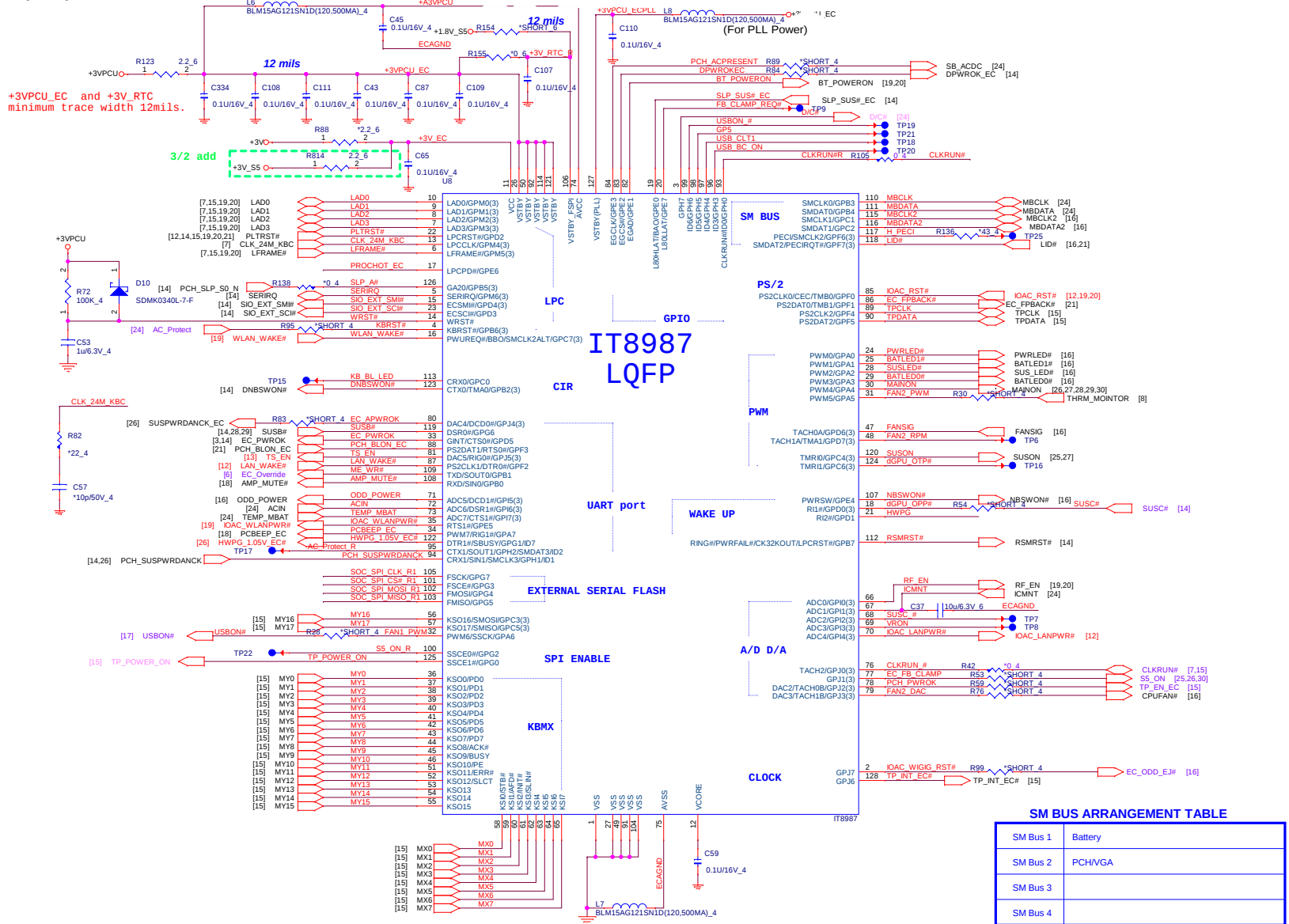
WLAN



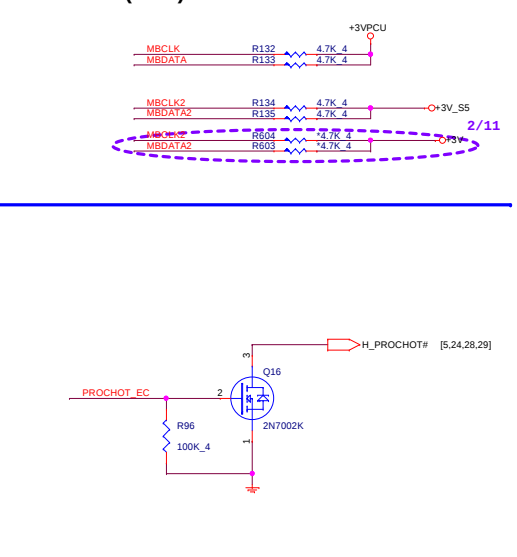
RF_EN_C C703 || *10p/50V 4



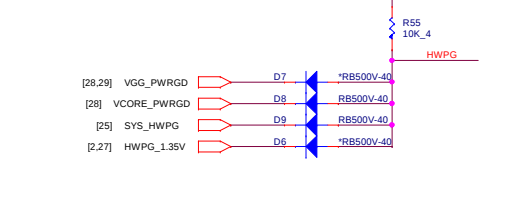
EC(KBC)



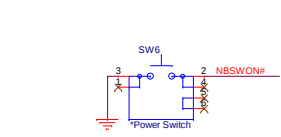
SM BUS PU(KBC)



HWPG(KBC)



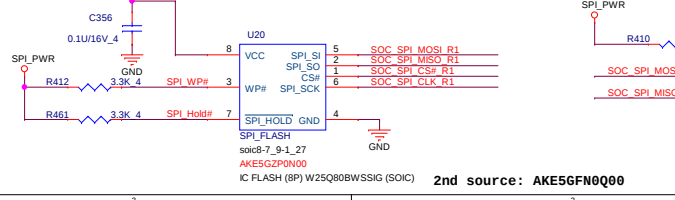
For test only



Reset SW (FSW)



SPI NOR FLASH



SM BUS ARRANGEMENT TABLE	
SM Bus 1	Battery
SM Bus 2	PCH/VGA
SM Bus 3	
SM Bus 4	

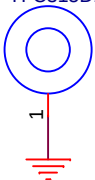
Quanta Computer Inc.
PROJECT : Z8AD
KBC IT8987

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		3A

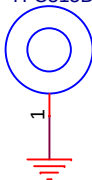
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2nd source: AKE5GFN0Q00

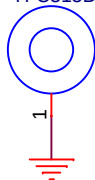
HOLE6
*H-C315D118P2



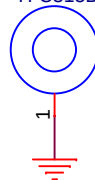
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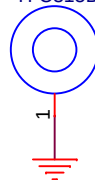
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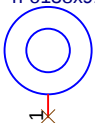
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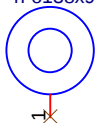
HOLE11
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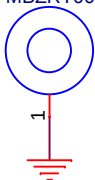
HOLE10
*h-o138x91d138x91n



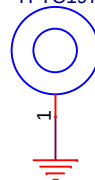
HOLE14
*h-o138x91d138x91n



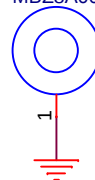
HOLE19
MBZRT001010



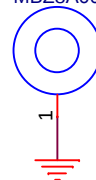
HOLE21
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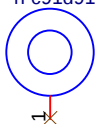
HOLE22
MBZ8A001010



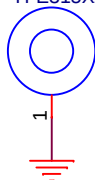
HOLE20
MBZ8A001010



HOLE12
*h-c91d91n



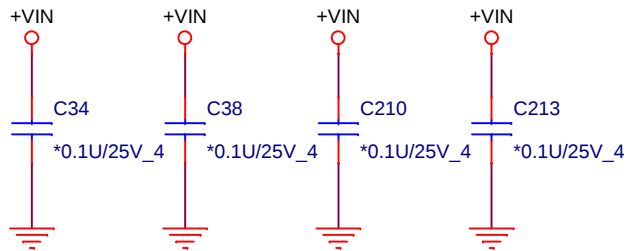
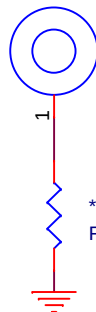
HOLE18
*H-E315X276D118P2



HOLE16
*H-C315D118P2



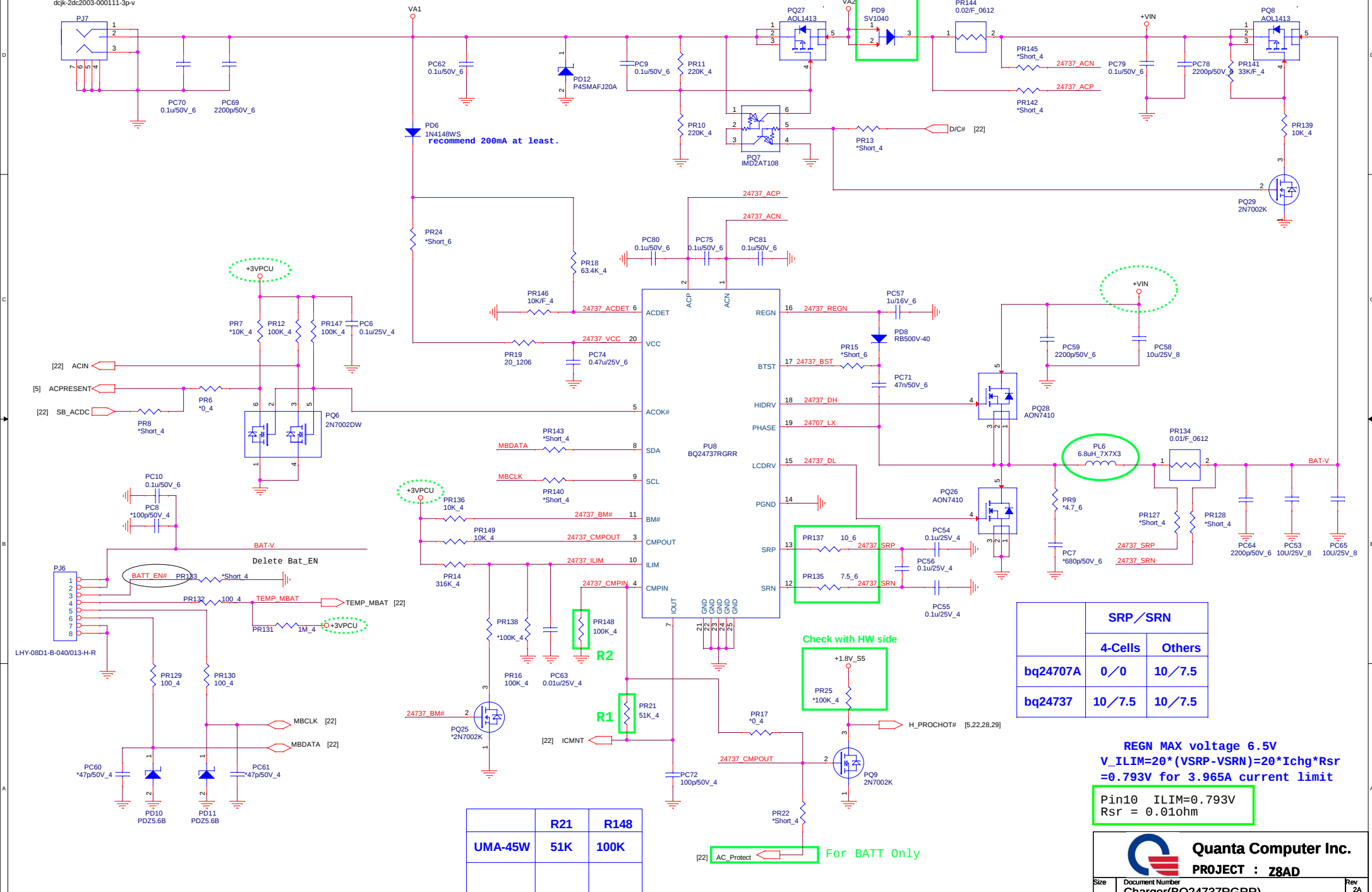
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HOLE7



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	Thermal / Hole	1A
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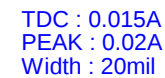
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dcjk-2dc2003-000111-3p-v

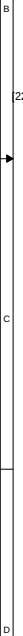


	SRP/SRN	
	4-Cells	Others
bq24707A	0/0	10/7.5
bq24737	10/7.5	10/7.5

REGN MAX voltage 6.5V
 $V_{ILIM}=20*(VSRP-VSRN)=20*I_{chg}*Rsr$
 $=0.793V$ for 3.965A current limit

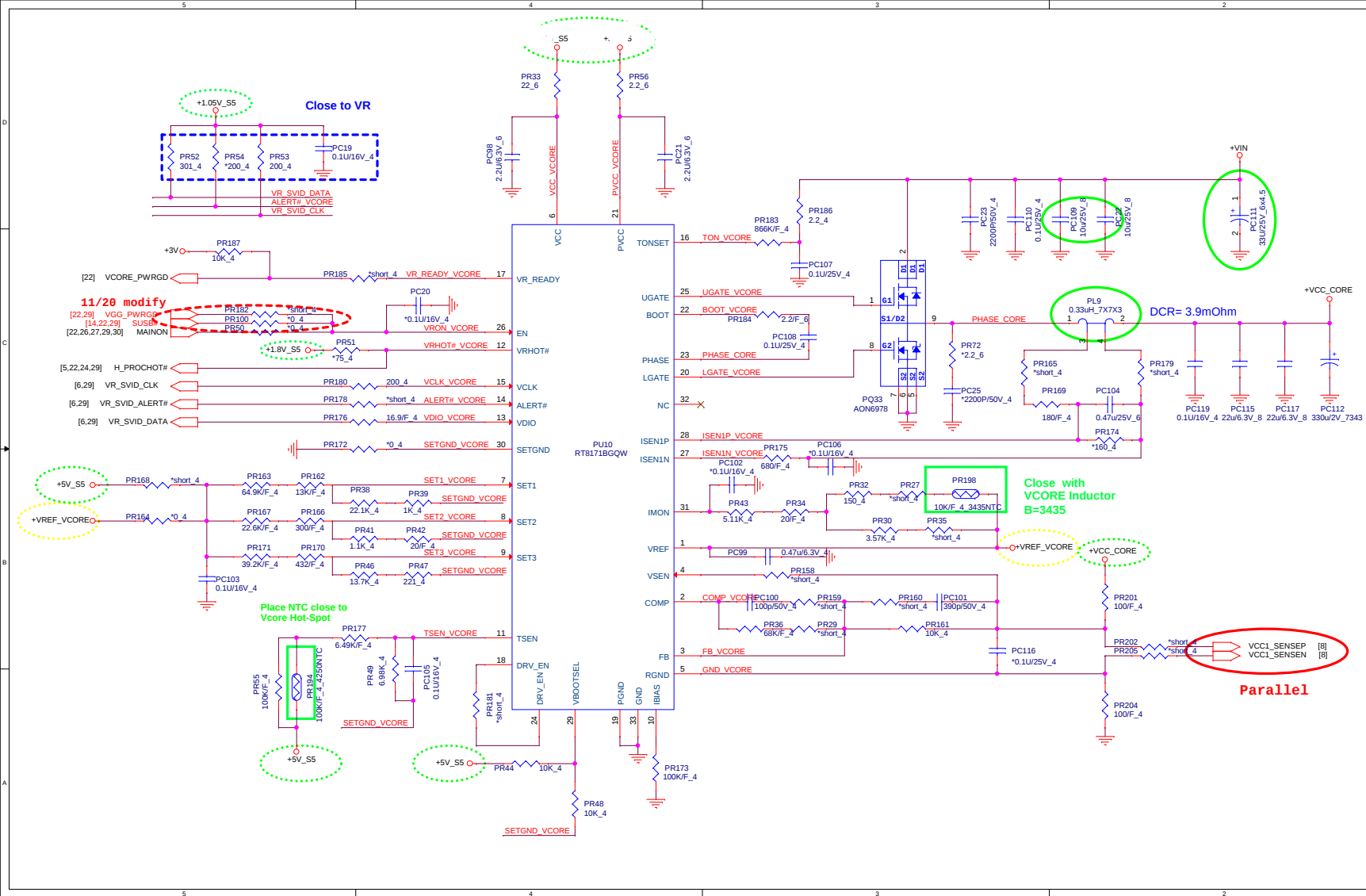
Pin10 ILIM=0.793V
Rsr = 0.01ohm





	S3	S5	+1.35VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3 (mainon off)	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

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VR 12.1

Braswell - VCC0+1 (1 Phase)

Icc TDC PL2 : TBD

Icc Max : 7A

OCP : 12.4A

Fsw : 800KHz

Vboot : 1V

VR address : 0

VCC0+1 L/L :

R_DC_LL : 0 mV/A

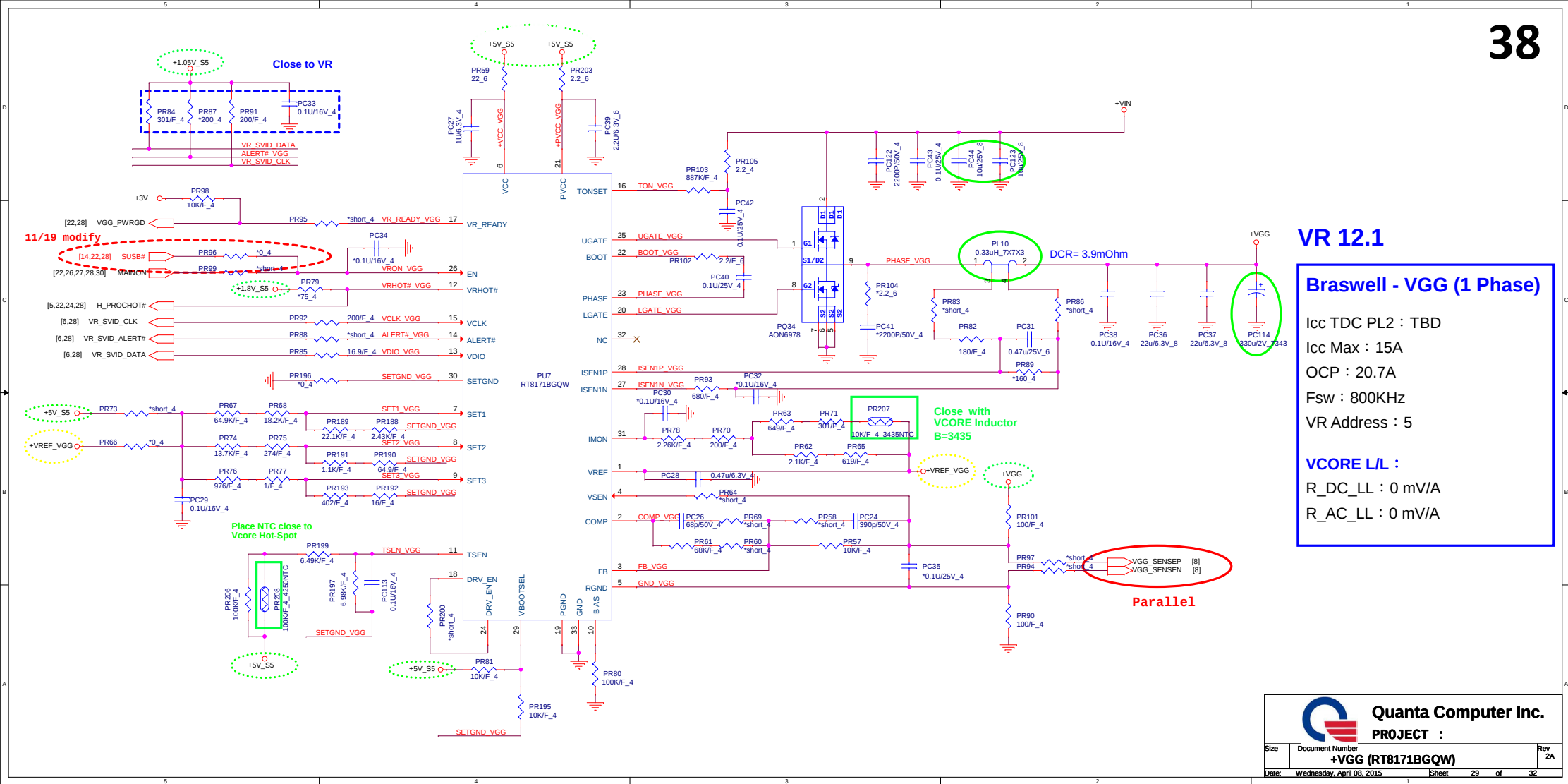
R_AC_LL : 0 mV/A

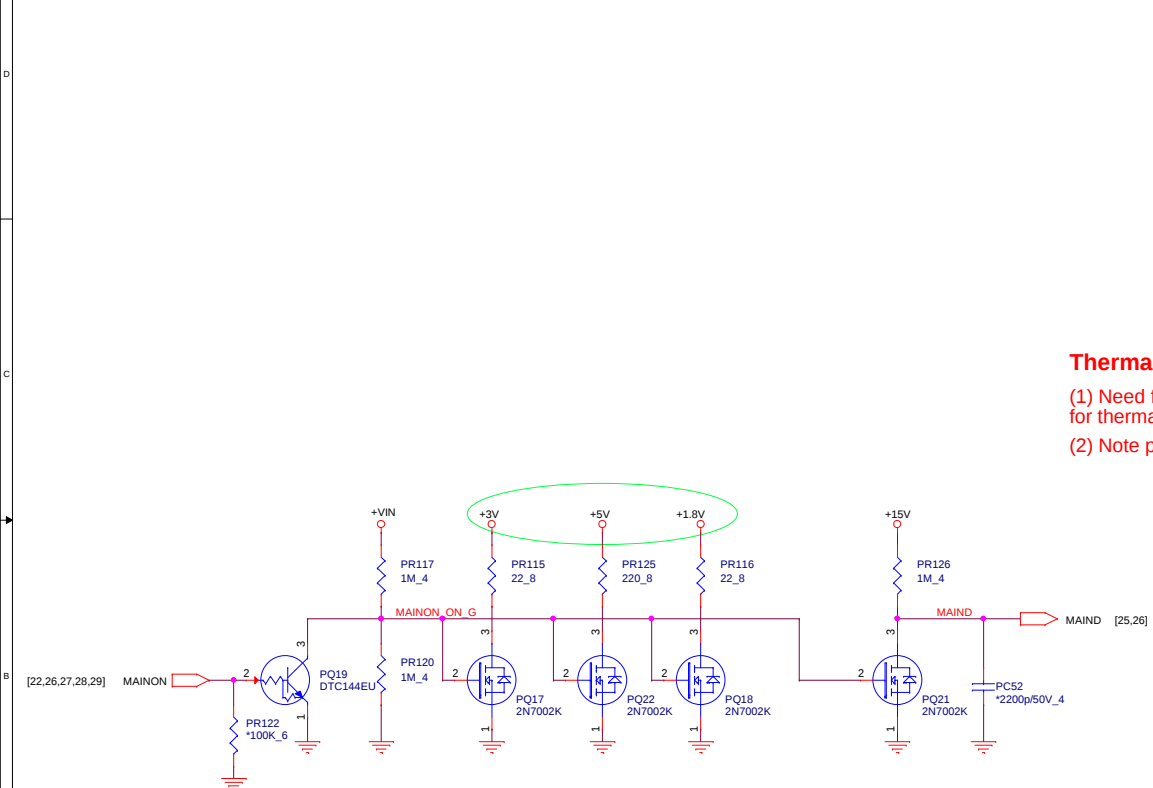


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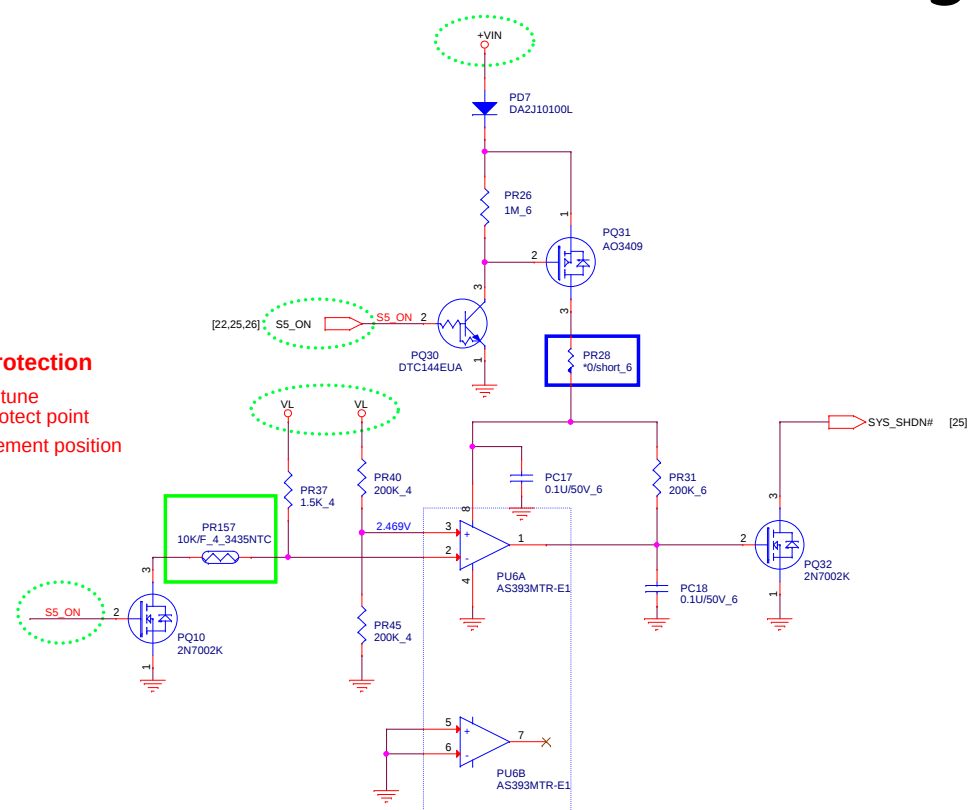
Size	Document Number	Rev
	VCC0+1 (RT8171BGQW)	2A
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Thermal Protection

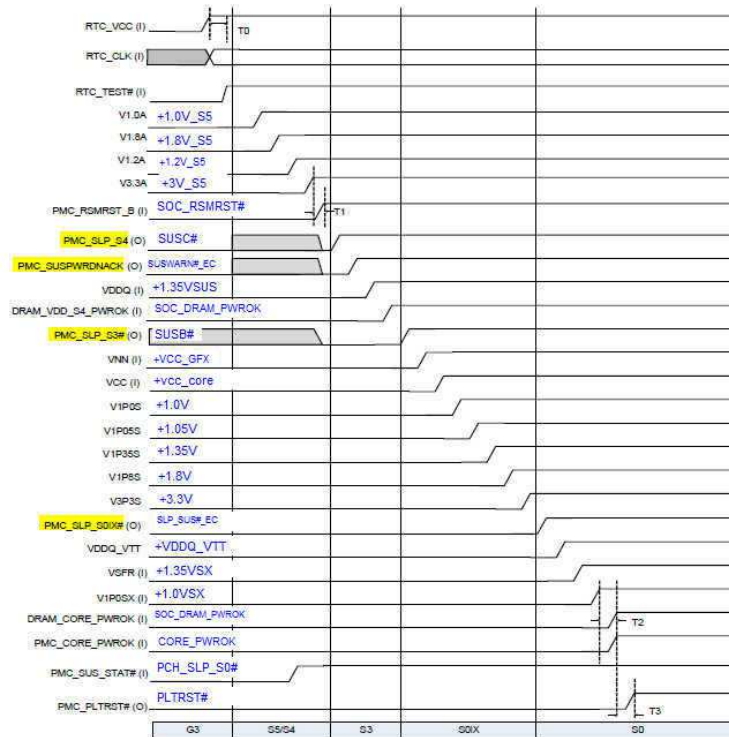
- (1) Need fine tune for thermal protect point
- (2) Note placement position



For EC control thermal protection (output 3.3V)

Bay Trail-M S4/S5 to S0 (Power up) Sequence

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Model	Version	CHANGE LIST
Z8AD	B	1225 page 6: change QP02_R337 not connect to SOC_KCB_SMI not & add R429 page 12: change U13 pin34 connect to GND & D4 PCBTEST not page 14: add Q24 & R22 page 19: D4 PCBTEST not & change C214 connect +VFCU & EMAC_WLANPWR & Q25 pin2 connect +3V_Mail_VDD page 20: D4 PCBTEST not page 31: add MAINSEN not & PR236 1229 page 6: add R261 connect to GND & R265, PMU_WPT_BURGLAR not page 14: add Q24 for Touch screen & U13 circuit for Intel WPT card page 19: add WPT_BURGLAR not & R264 page 20: add SL2_239 not & PR237 & PR238 AMASINCN not 106 page 6: Move SOC_KCB_SMI to SATA_GP(pin A03) page 14: add R261 page 15: add R265&R262C294&R266 page 16: D4 Q25,R279 page 21: D4 Q279 & add Q25,R292&R293&R296 108 page 3: D4 R215 page 14: D4 R261 page 8: D4 R499,R488 & add C295,C296 page 31: D4 R262
	C	1225 page 6: add board ID 0 & R800,R801 page 22: add R802, R298 & R299 AD4 R109 30 page 5: add OSD circuit OSD_PRESENT connect to SATA_LEDW (134D A13) & Add SSD ID at pin A27 (SATA_0P2) Add R810,R811 page 22: add R813 page 16: add R812,C893 ACOD_PRESENT not, SSD ID not page 22: add R814 page 6: D4 R265 & Add TP 24 page 14: D4 U27,R265,R262,C293 page 19: D4 R264 & Add TP 47 page 15: Add R815,R816,R817,C894,C895,C896,C897 page 16: Add R815,R816,R817,C896,C897,C700,C702 page 19: Add R821,R822,C894,C895

DOC NO.

PROJECT MODEL :

PART NUMBER:

APPROVED BY:

DRAWING BY:

DATE:

REVISION:



Quanta Computer Inc.

PROJECT : Z8AD

Change list

Version: 2023-01-01